

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document
Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH
Nvidia N13P GS/GL

2011-12-24

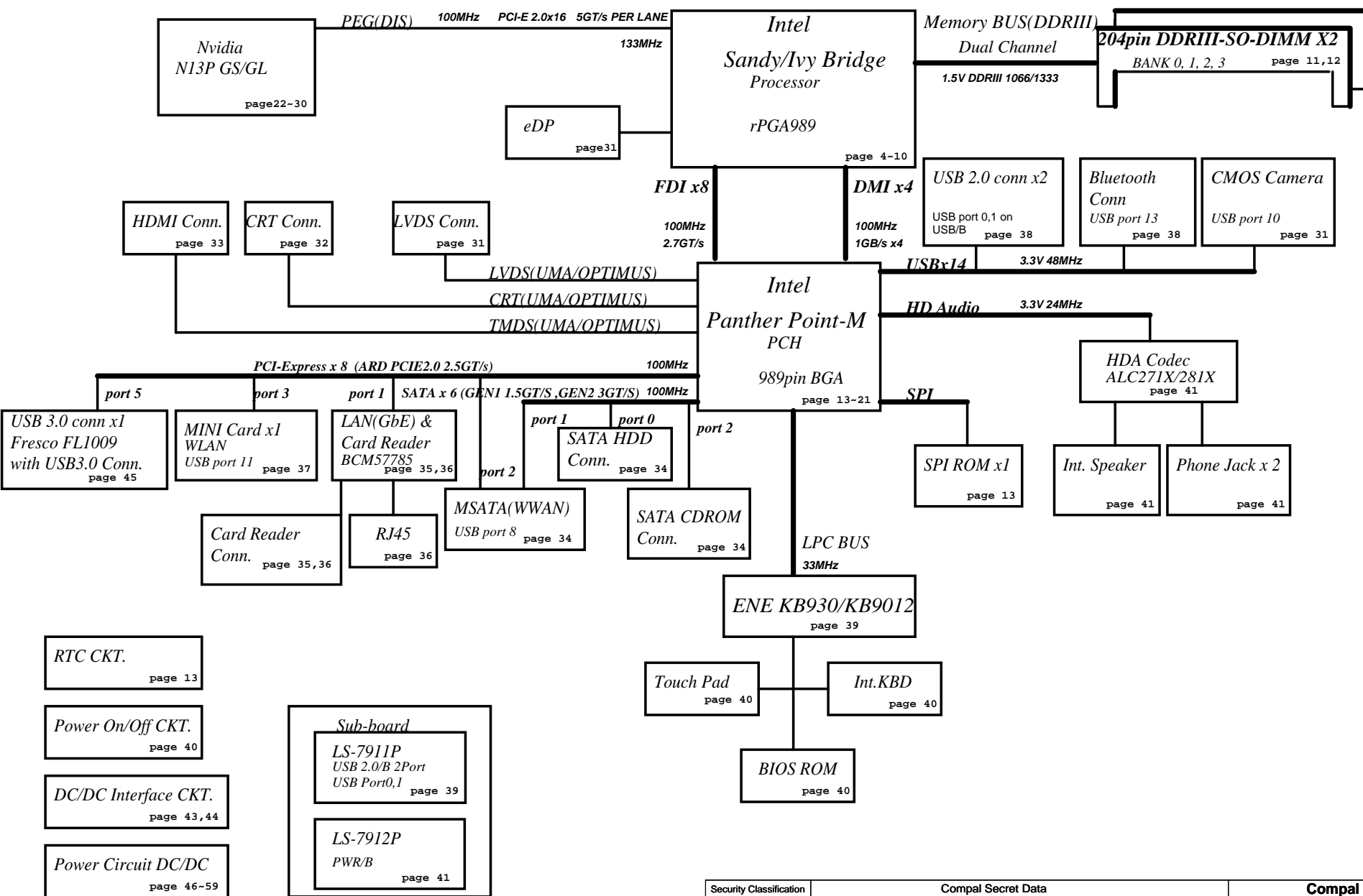
REV : 0 . 2

MB PCB	
Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B



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				Custom	4019ID	B
				Date:	Friday, January 06, 2012	Sheet 1 of 60

Fan Control
page 42



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				Date	Friday, January 06, 2012
				Sheet	2 of 60

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BT & USB30 & USB20 Config

OPTMIUS SKU:DIS@ N13P-GL:GL@ N13P-GS:GS@ N13P-GF108_ES4:GF108@
BT SKU:BT@
internal USB SKU: PUSB@ DIS USB30 SKU:DUSB@
eDP SKU: EDP@
LVDS SKU: LVDS@
EC 930 SKU: 930@ EC 9012 SKU: 9012@
PCH HM65: HM65@ PCH HM76: HM76@
Win8: WIN8@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@

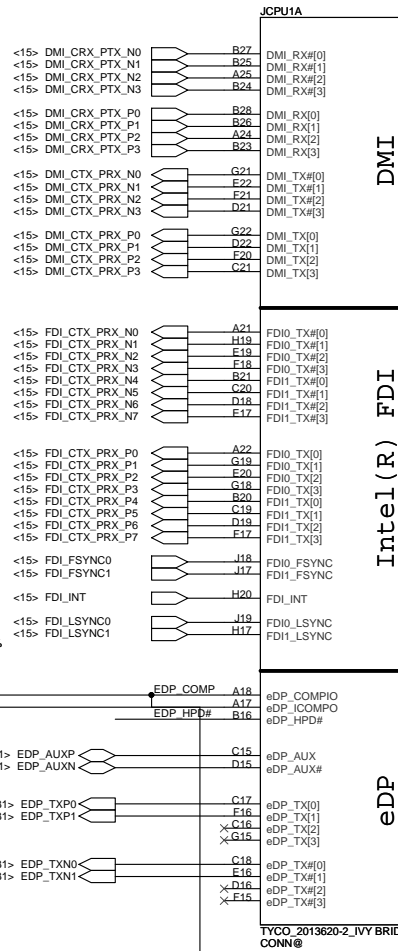
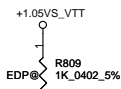
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
		5	
EHCI2	UHCI3	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI4	9	
		10	Camera
		11	BlueTooth
	UHCI6	12	
		13	

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				4019ID	B
				Date: Friday, January 06, 2012	Sheet 3 of 60

eDP_COMPIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPIO=4mils,
EDP_ICOMPO=12mils,
and both length less than 500 mils...
should not be left floating
,even if disable eDP function...

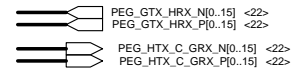
Add eDP circuit



PCI EXPRESS* - GRAPHICS

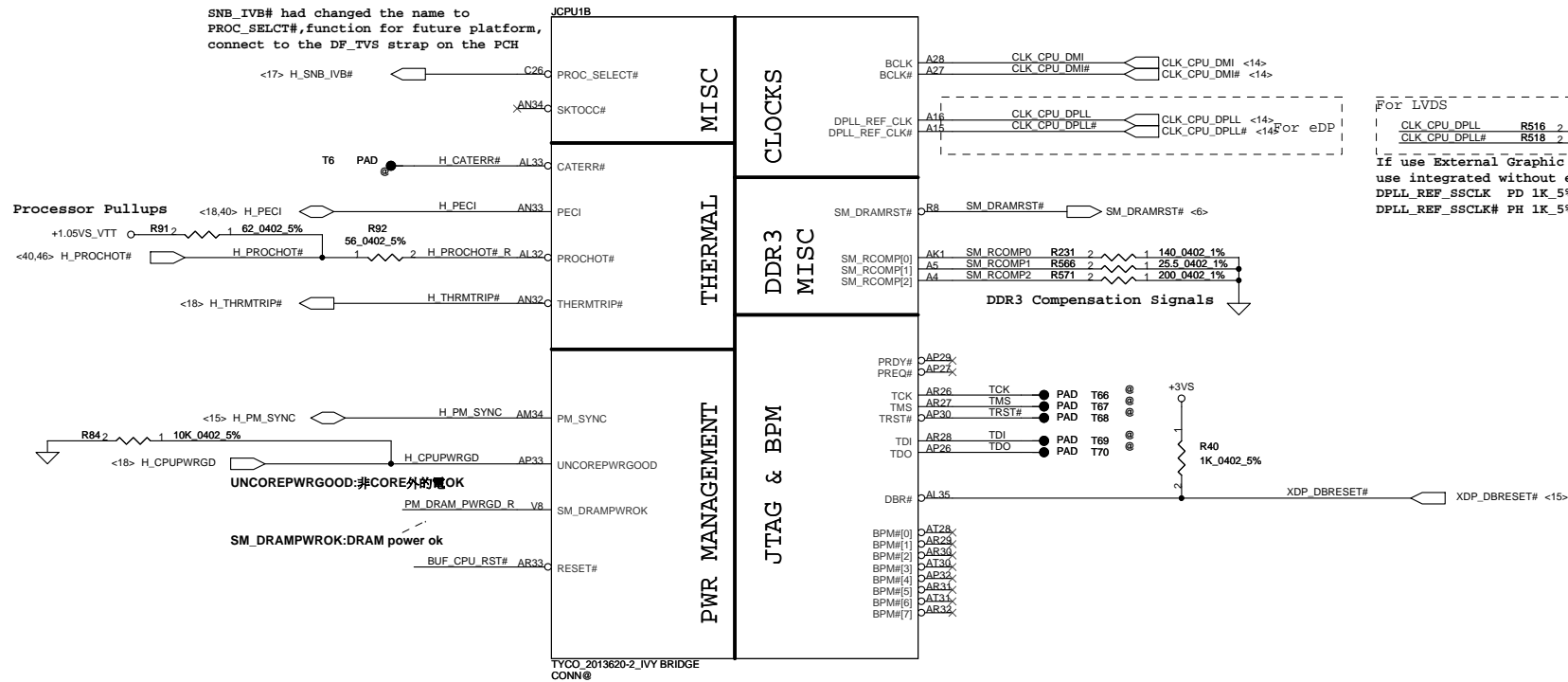
PEG_ICOMPI	J22	PEG_COMP	
PEG_ICOMPO	J21		
PEG_RCOMPO	H22		
PEG_RX[0]	K33	PEG GTX C HRX N15 C46	1
PEG_RX[1]	M35	PEG GTX C HRX N14 C49	1
PEG_RX[2]	L34	PEG GTX C HRX N13 C51	1
PEG_RX[3]	J35	PEG GTX C HRX N12 C53	1
PEG_RX[4]	J32	PEG GTX C HRX N11 C60	1
PEG_RX[5]	H34	PEG GTX C HRX N10 C71	1
PEG_RX[6]	H31	PEG GTX C HRX N9 C75	1
PEG_RX[7]	G33	PEG GTX C HRX N8 C82	1
PEG_RX[8]	G30	PEG GTX C HRX N7 C92	1
PEG_RX[9]	F35	PEG GTX C HRX N6 C93	1
PEG_RX[10]	E34	PEG GTX C HRX N5 C102	1
PEG_RX[11]	E32	PEG GTX C HRX N4 C111	1
PEG_RX[12]	D33	PEG GTX C HRX N3 C113	1
PEG_RX[13]	D31	PEG GTX C HRX N2 C125	1
PEG_RX[14]	B33	PEG GTX C HRX N1 C129	1
PEG_RX[15]	C32	PEG GTX C HRX N0 C144	1
PEG_RX[0]	J33	PEG GTX C HRX P15 C47	1
PEG_RX[1]	L35	PEG GTX C HRX P14 C49	1
PEG_RX[2]	K34	PEG GTX C HRX P13 C52	1
PEG_RX[3]	H35	PEG GTX C HRX P12 C56	1
PEG_RX[4]	H32	PEG GTX C HRX P11 C66	1
PEG_RX[5]	G34	PEG GTX C HRX P10 C68	1
PEG_RX[6]	F31	PEG GTX C HRX P9 C81	1
PEG_RX[7]	F33	PEG GTX C HRX P8 C86	1
PEG_RX[8]	F30	PEG GTX C HRX P7 C89	1
PEG_RX[9]	F35	PEG GTX C HRX P6 C100	1
PEG_RX[10]	E33	PEG GTX C HRX P5 C105	1
PEG_RX[11]	E32	PEG GTX C HRX P4 C106	1
PEG_RX[12]	D34	PEG GTX C HRX P3 C117	1
PEG_RX[13]	E31	PEG GTX C HRX P2 C119	1
PEG_RX[14]	C33	PEG GTX C HRX P1 C129	1
PEG_RX[15]	B32	PEG GTX C HRX P0 C138	1
PEG_TX[0]	M29	PEG HTX GRX N15 C516	1
PEG_TX[1]	M32	PEG HTX GRX N14 C520	1
PEG_TX[2]	M31	PEG HTX GRX N13 C529	1
PEG_TX[3]	L32	PEG HTX GRX N12 C534	1
PEG_TX[4]	L29	PEG HTX GRX N11 C538	1
PEG_TX[5]	K31	PEG HTX GRX N10 C540	1
PEG_TX[6]	K28	PEG HTX GRX N9 C542	1
PEG_TX[7]	J30	PEG HTX GRX N8 C544	1
PEG_TX[8]	J28	PEG HTX GRX N7 C546	1
PEG_TX[9]	H29	PEG HTX GRX N6 C548	1
PEG_TX[10]	G27	PEG HTX GRX N5 C550	1
PEG_TX[11]	E29	PEG HTX GRX N4 C552	1
PEG_TX[12]	E27	PEG HTX GRX N3 C554	1
PEG_TX[13]	D28	PEG HTX GRX N2 C556	1
PEG_TX[14]	F26	PEG HTX GRX N1 C558	1
PEG_TX[15]	E25	PEG HTX GRX N0 C560	1
PEG_TX[0]	M28	PEG HTX GRX P15 C515	1
PEG_TX[1]	M33	PEG HTX GRX P14 C528	1
PEG_TX[2]	M30	PEG HTX GRX P13 C533	1
PEG_TX[3]	L31	PEG HTX GRX P12 C536	1
PEG_TX[4]	L28	PEG HTX GRX P11 C539	1
PEG_TX[5]	K30	PEG HTX GRX P10 C541	1
PEG_TX[6]	K27	PEG HTX GRX P9 C543	1
PEG_TX[7]	J29	PEG HTX GRX P8 C545	1
PEG_TX[8]	J27	PEG HTX GRX P7 C547	1
PEG_TX[9]	H28	PEG HTX GRX P6 C549	1
PEG_TX[10]	G28	PEG HTX GRX P5 C551	1
PEG_TX[11]	E28	PEG HTX GRX P4 C553	1
PEG_TX[12]	E28	PEG HTX GRX P3 C555	1
PEG_TX[13]	D27	PEG HTX GRX P2 C557	1
PEG_TX[14]	E26	PEG HTX GRX P1 C559	1
PEG_TX[15]	D25	PEG HTX GRX P0 C561	1

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils,trace width=4mils
PEG_ICOMPO signals should be routed with - max
length = 500 mils,trace width=12mils
spacing =15mils



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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		Document Number	40191D
		Date	Friday, January 06, 2012
		Sheet	4 of 60



For LVDS

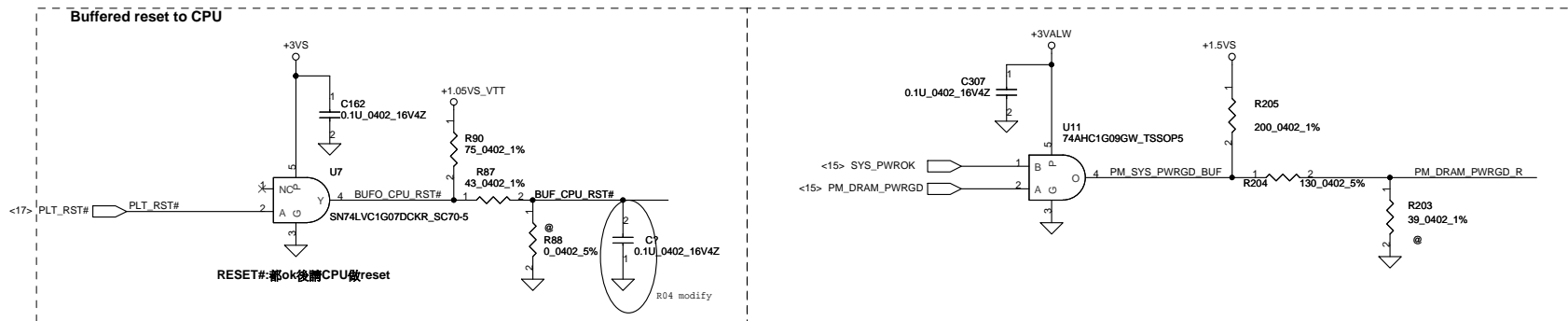
CLK CPU DPLL R516 2 LVDS@ 1K 0402_5%

CLK CPU DPLL# R518 2 LVDS@ 1K 0402_5%

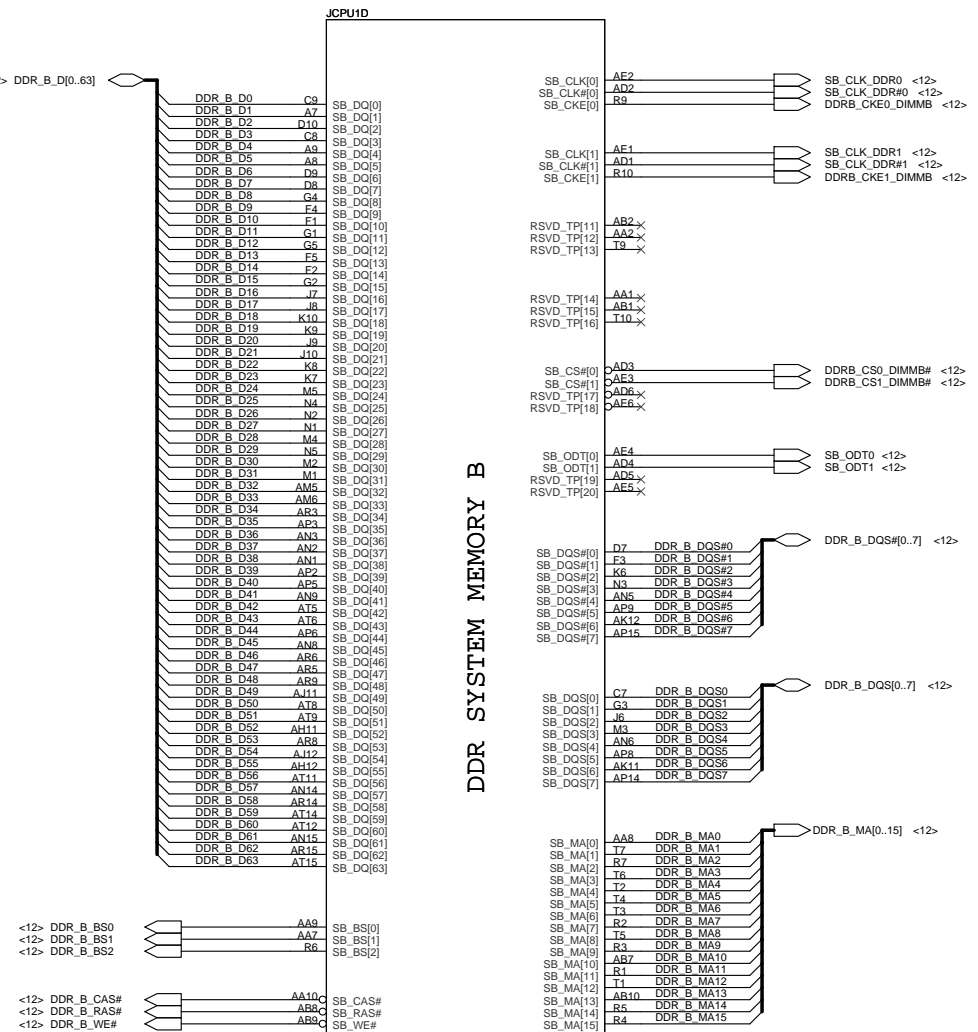
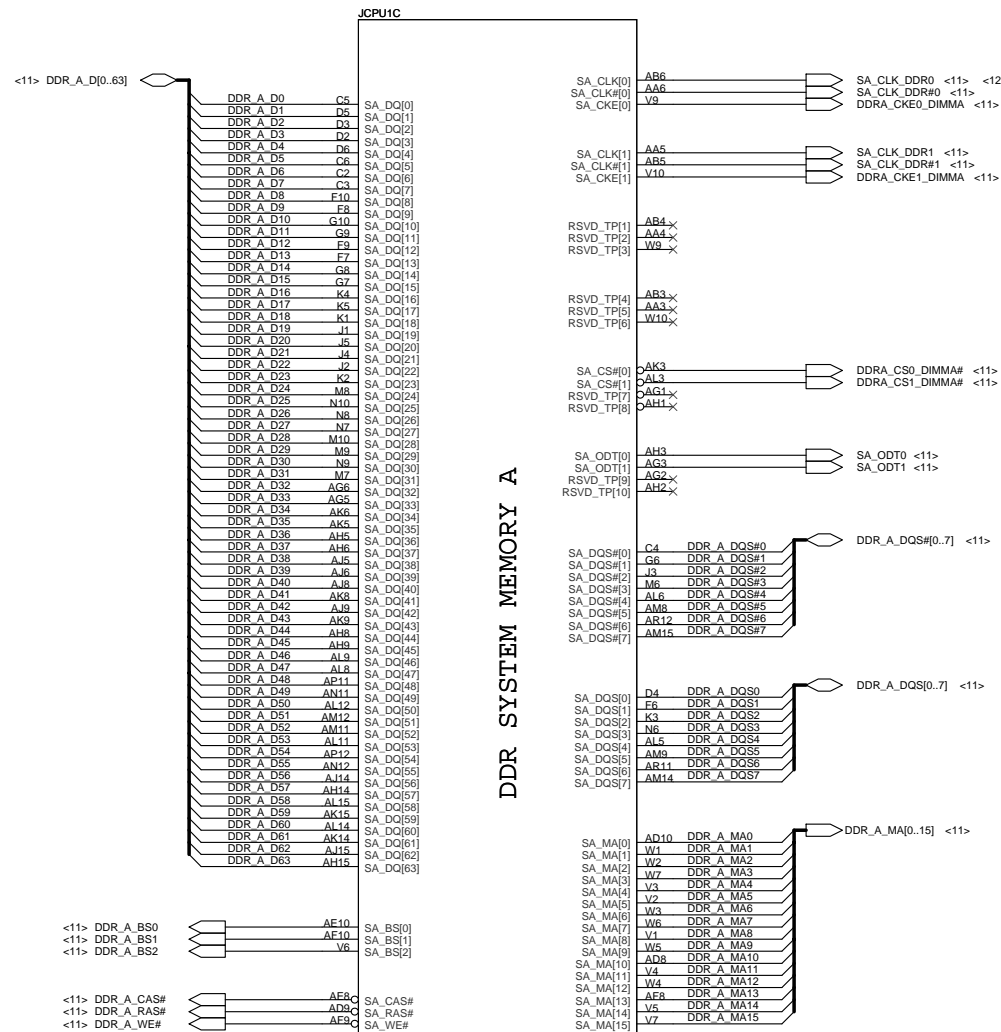
If use External Graphic or use integrated without eDP

DPLL_REF_SSCLK PD 1K_5% to GND

DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

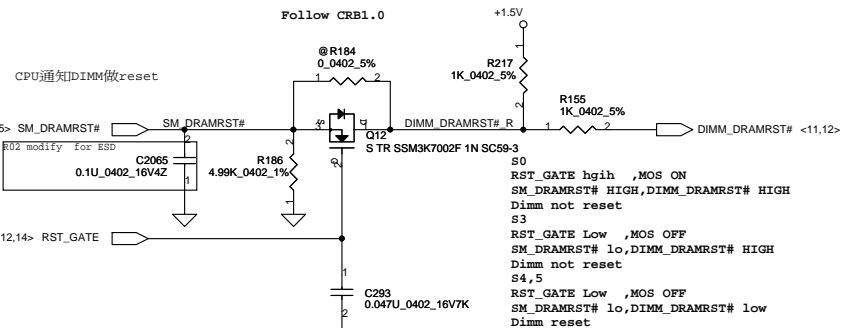


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						Date:		Friday, January 06, 2012		Sheet 5 of (6)	
						Custom					



DDR SYSTEM MEMORY A

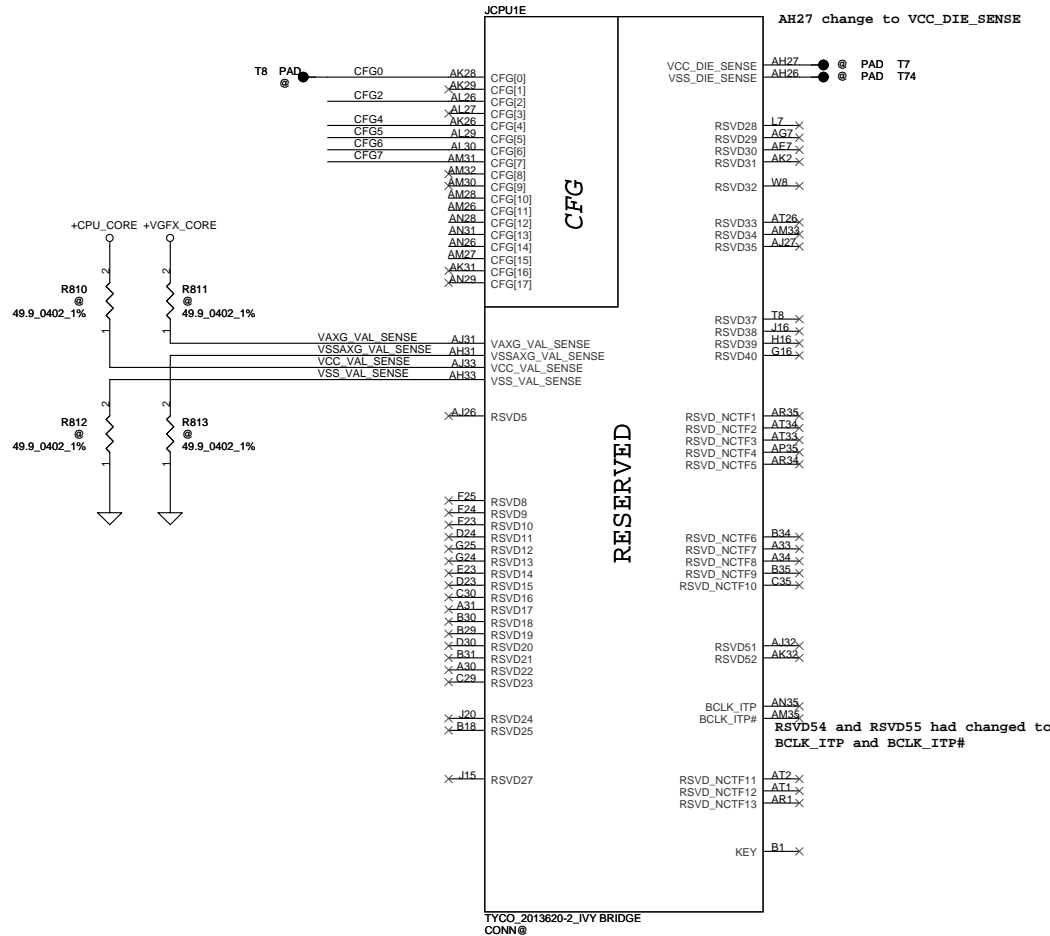
DDR SYSTEM MEMORY B



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				4019ID
				Rev B
				Date: Friday, January 06, 2012
				Sheet 6 of 60

CFG Straps for Processor

AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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				Date	Friday, January 06, 2012
				Sheet	7 of 60
				Rev	B

SV type CPU JCPU1F

+CPU_CORE
QC 53A
DC 53A

VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
VCC51
VCC52
VCC53
VCC54
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VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
VCC76
VCC77
VCC78
VCC79
VCC80
VCC81
VCC82
VCC83
VCC84
VCC85
VCC86
VCC87
VCC88
VCC89
VCC90
VCC91
VCC92
VCC93
VCC94
VCC95
VCC96
VCC97
VCC98
VCC99
VCC100

POWER

PEG AND DDR

CORE SUPPLY

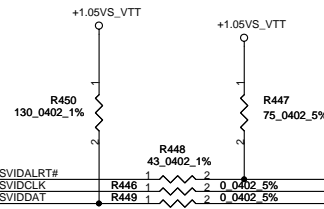
SVID

SENSE LINES

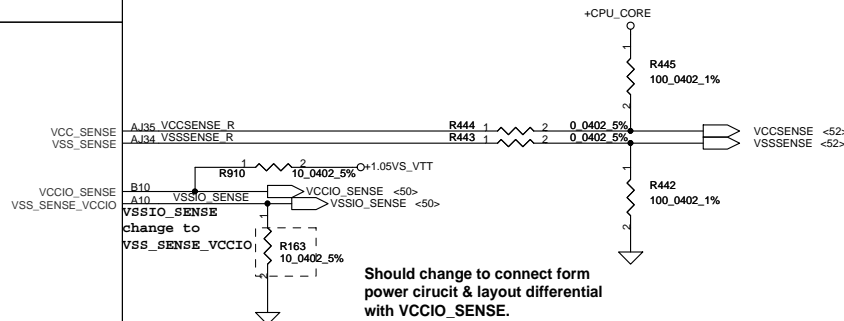
8.5A

+1.05VS_VTT

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AC10
VCCIO4 Y10
VCCIO5 U10
VCCIO6 P10
VCCIO7 L10
VCCIO8 J14
VCCIO9 J13
VCCIO10 J12
VCCIO11 H14
VCCIO12 H14
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
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VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

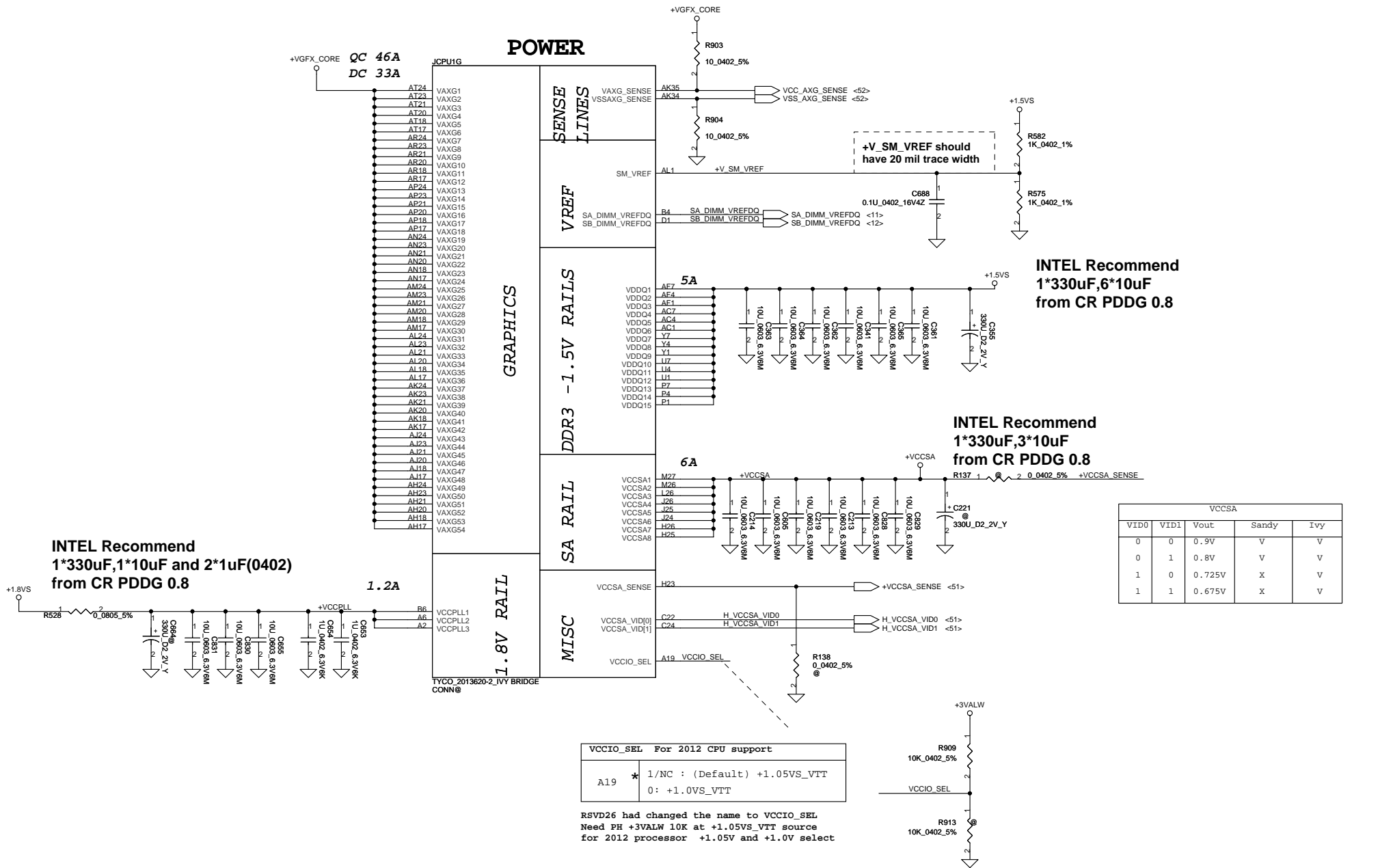


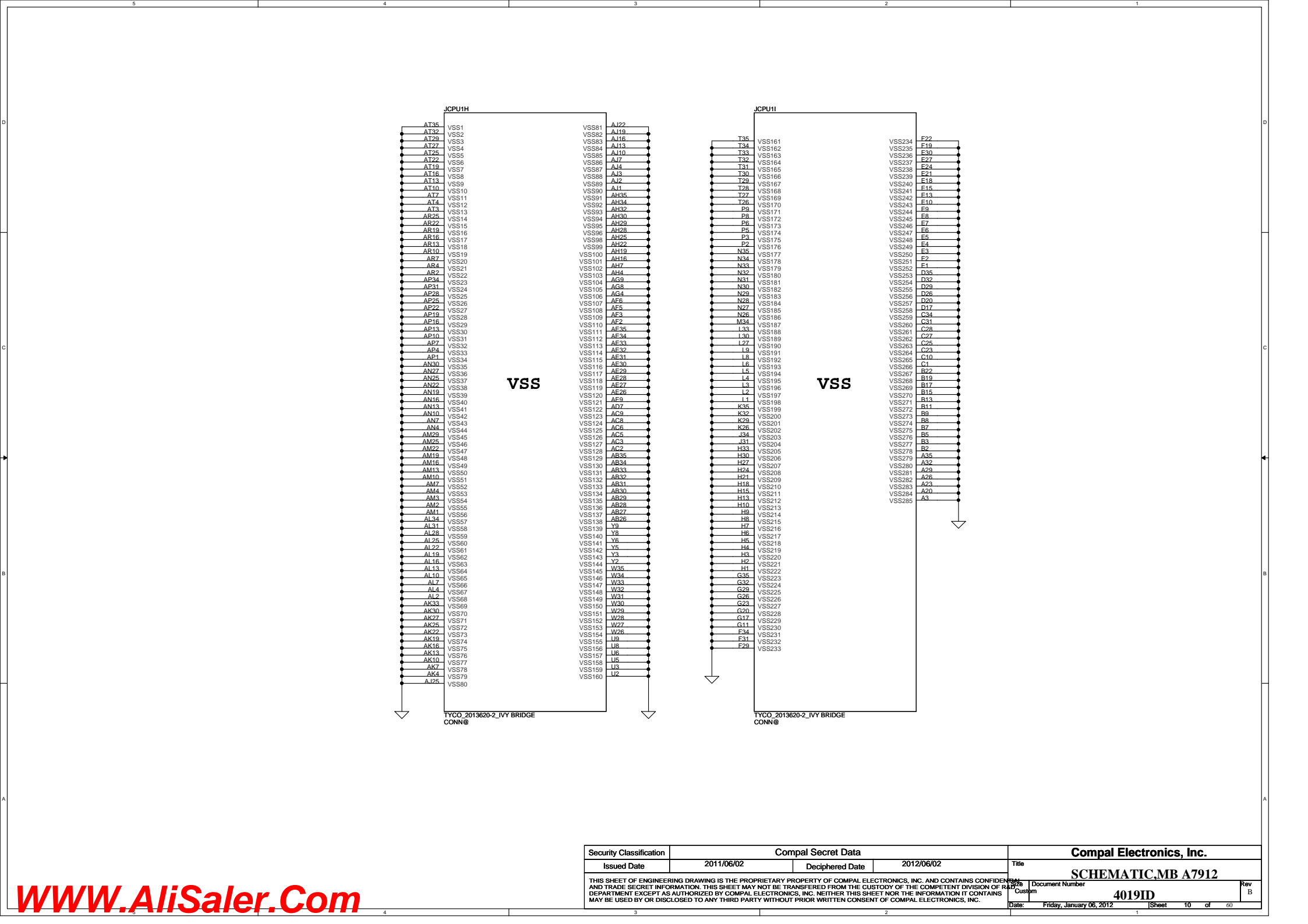
Place the PU resistors close to CPU



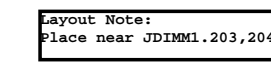
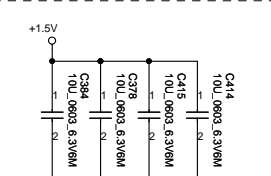
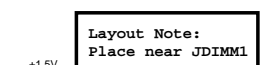
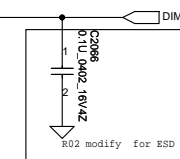
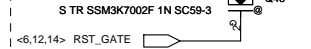
TYCO_2013620-2_IVY BRIDGE CONN@

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				Date	Friday, January 06, 2012	Sheet 8 of 60





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				Date	Friday, January 06, 2012
				Sheet	10 of 60
				Rev	B



DIMM_1 Reserve H:8mm

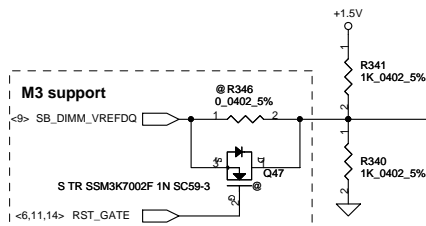
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SCHEMATIC MB A7912

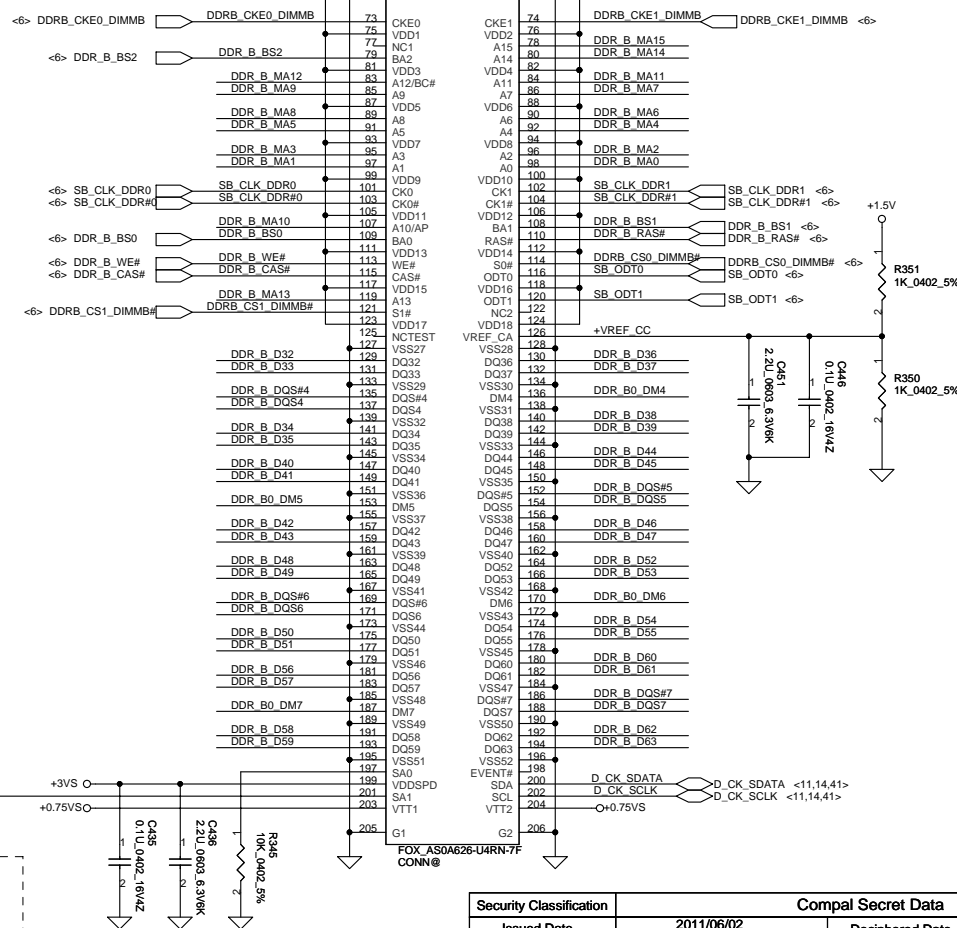
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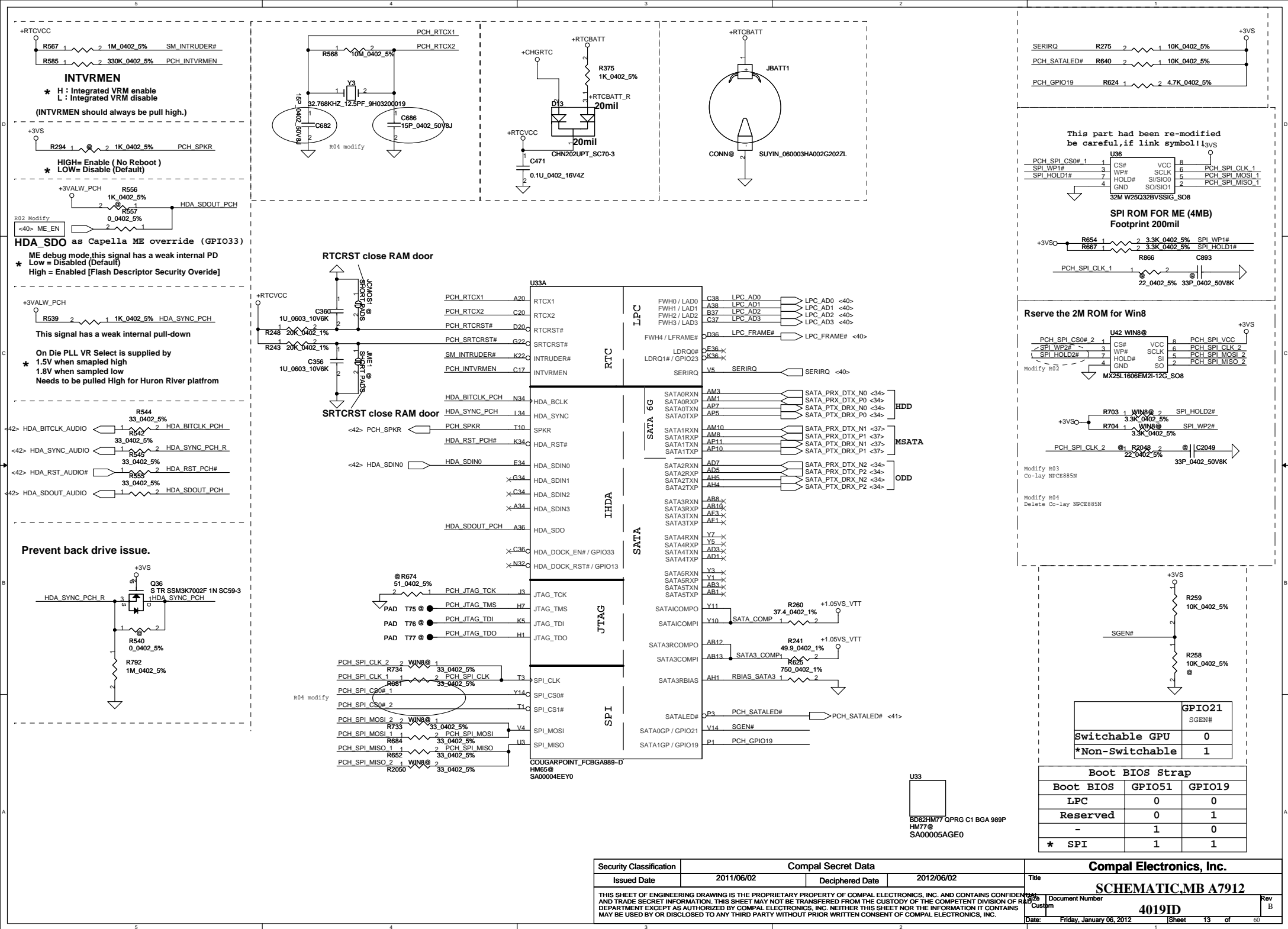
Rev B

Date: Friday, January 06, 2012 Sheet 11 of 60

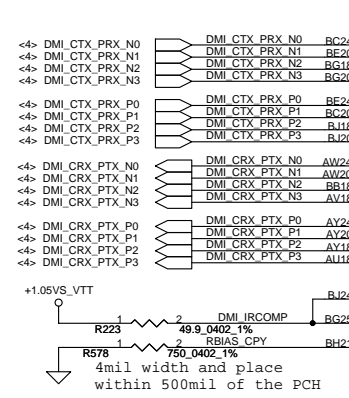
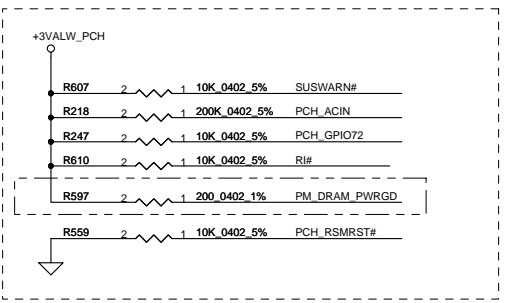


All VREF traces should have 10 mil trace width

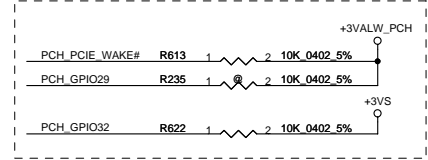
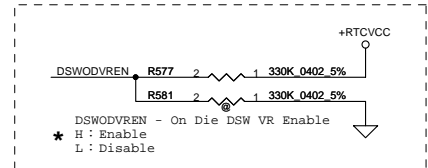
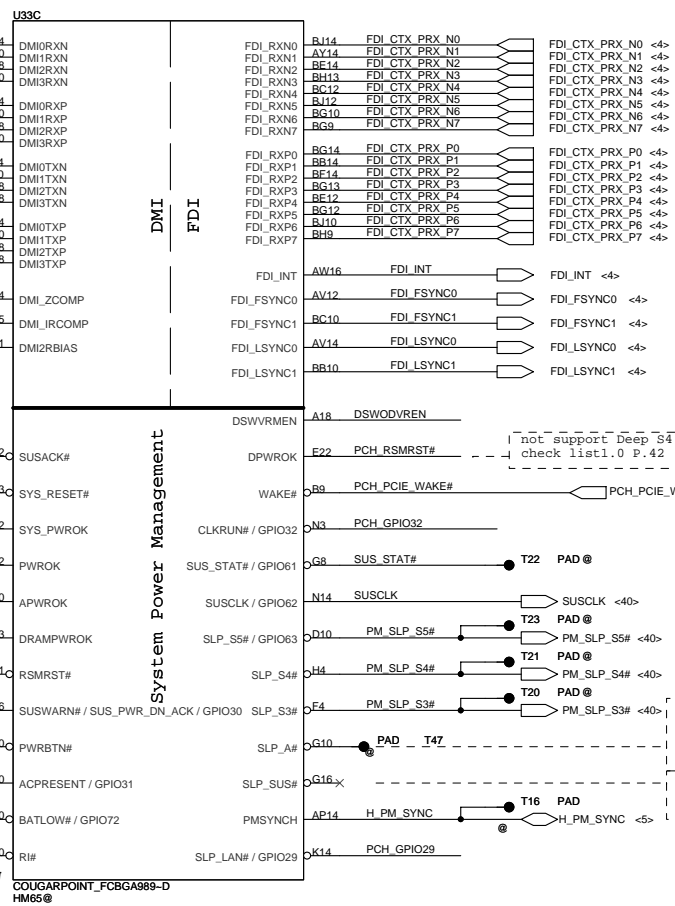
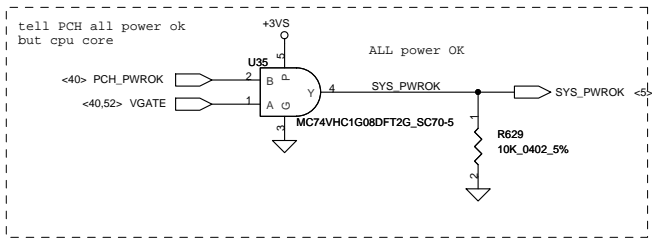
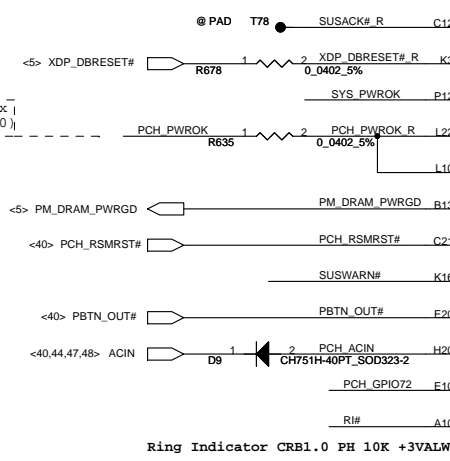








not support AMT APWROK can mux
with PWROK (check list1.0 P.40)



Can be left NC
when IAMT is not
support on the
platform
not support
Deep S4,S5 can NC
PCH EDS1.2 P.74

<40> ENBKLT ENBKLT R532 2 0.0402_5% IGPU_BKLT_EN

+3VS
R174 1 2.2K_0402_5% CTRL_CLK
R158 1 2.2K_0402_5% CTRL_DATA
R156 1 2.2K_0402_5% PCH_LCD_CLK
R157 1 2.2K_0402_5% PCH_LCD_DATA

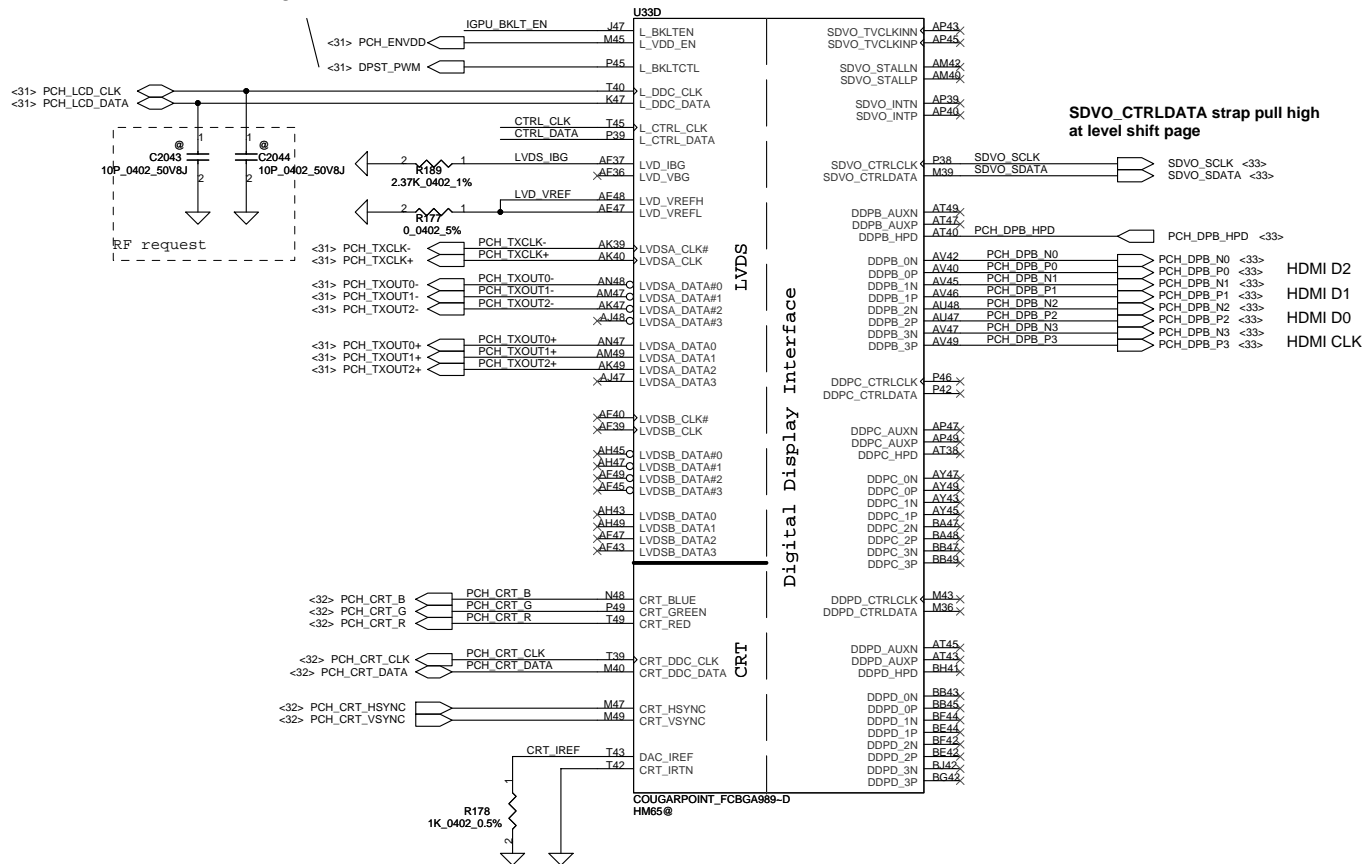
+3VS
R521 1 2.2K_0402_5% PCH_CRT_CLK
R522 1 2.2K_0402_5% PCH_CRT_DATA

R534 1 2.150_0402_1% PCH_CRT_B
R533 1 2.150_0402_1% PCH_CRT_G
R535 1 2.150_0402_1% PCH_CRT_R

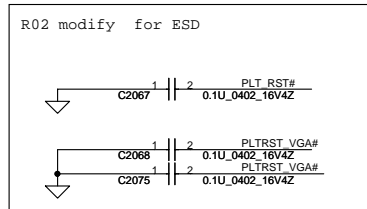
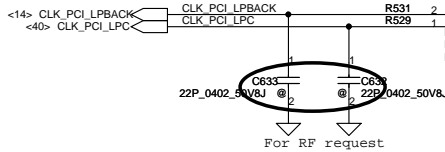
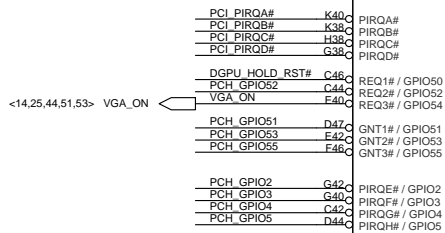
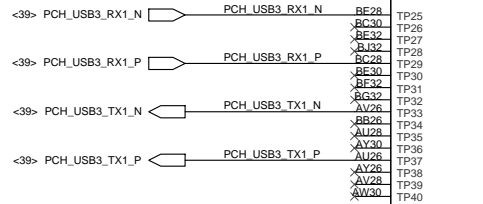
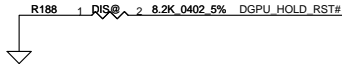
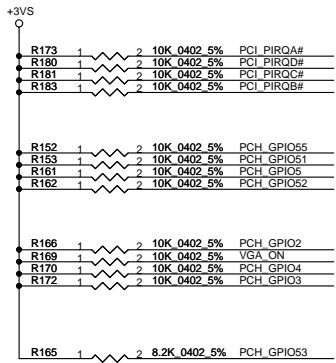
R02 Modify

C2076 1 1U_0402_6.3V6K PCH_DPB_HPD

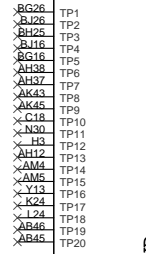
Pull high at LVDS conn side.



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U33E



RSVD

PCI

USB

CMOS.Camera (LVDS)

BlueTooth

Within 500 mils

R05 Modify

USB_OC0#

SMIB

PLT_RST#

DGPU_HOLD_RST#

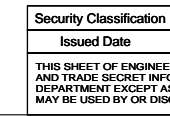
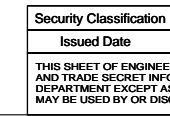
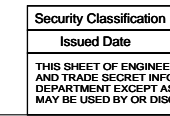
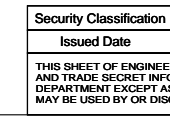
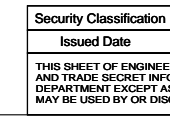
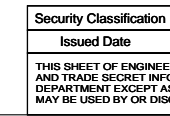
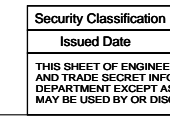
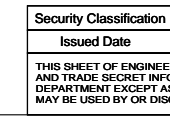
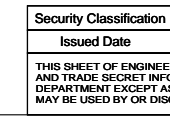
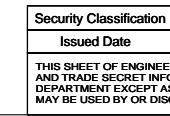
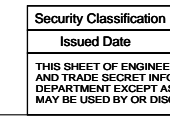
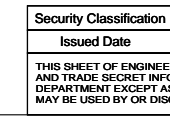
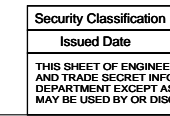
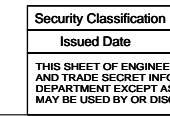
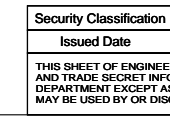
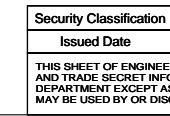
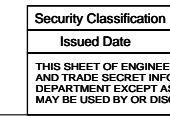
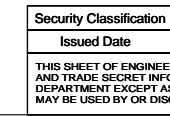
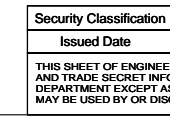
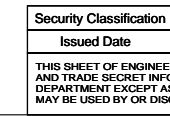
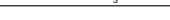
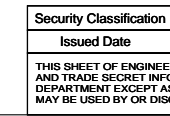
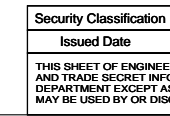
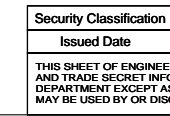
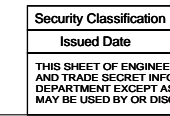
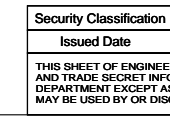
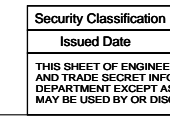
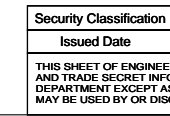
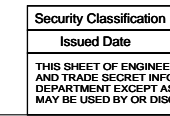
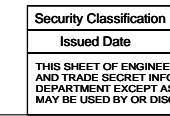
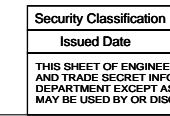
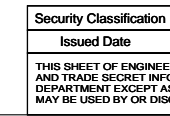
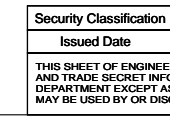
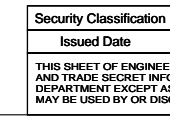
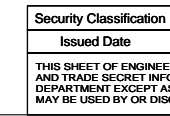
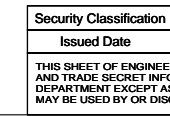
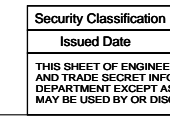
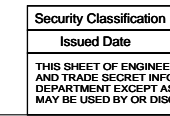
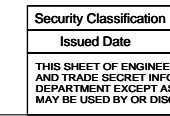
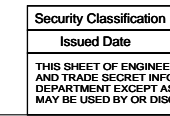
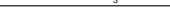
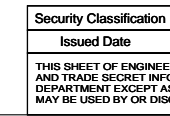
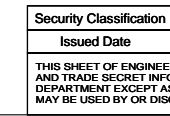
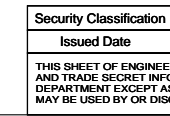
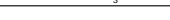
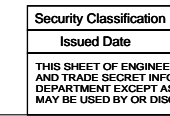
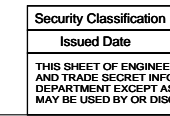
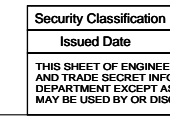
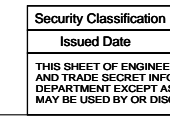
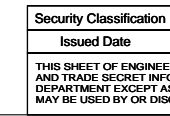
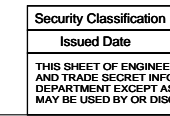
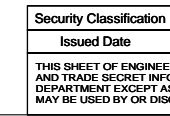
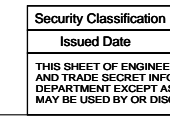
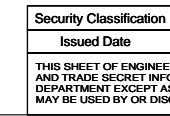
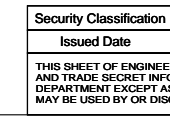
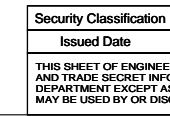
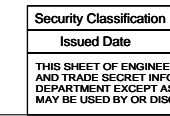
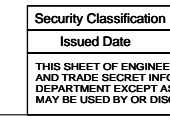
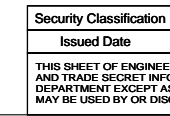
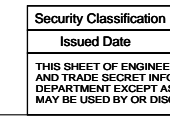
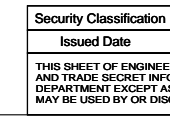
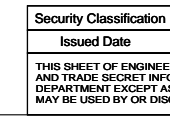
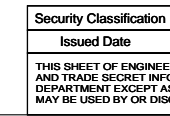
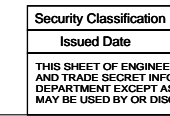
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PLTRST_VGA#

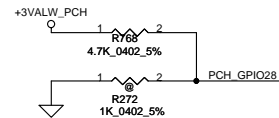
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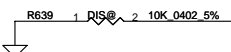
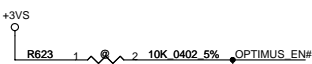
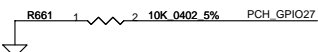
PLTRST_VGA#



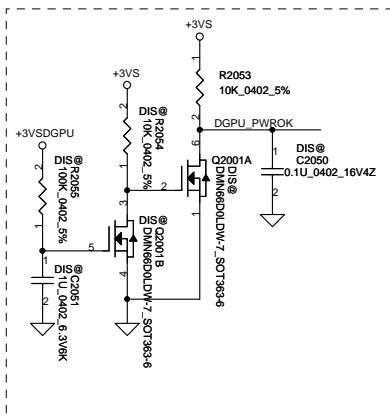
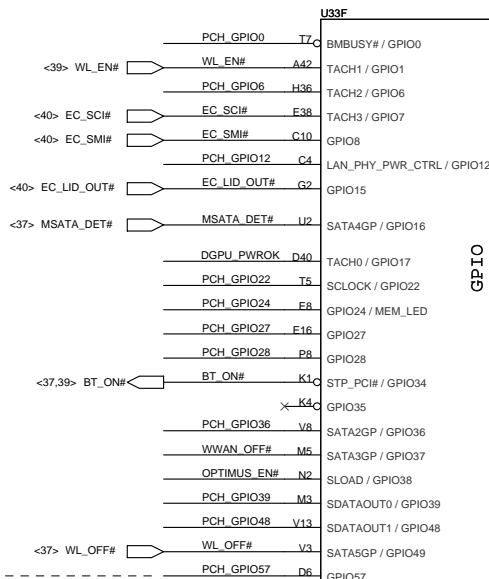
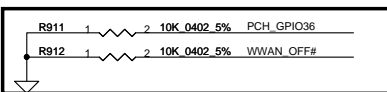
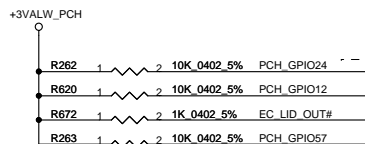
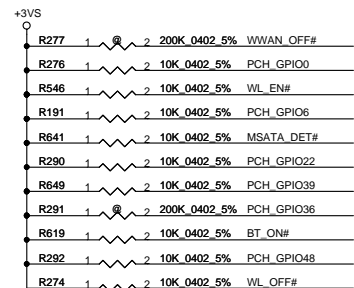
- * H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70



	GPI038 OPTIMUS_EN#
OPTIMUS	0
DIS Only	1



```

|GPIO24 Unmultiplexed-----
|NOTE: GPIO24 configuration
|register bits are not cleared by
|CF9h reset event.

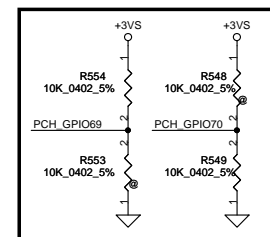
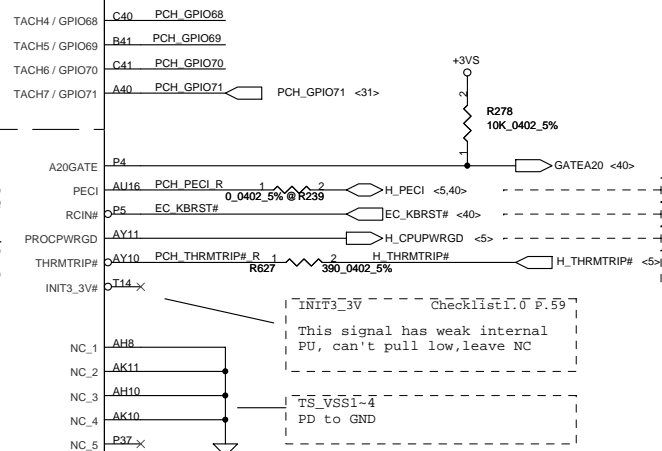
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CRB1.0 PH10K to +3VALW

```

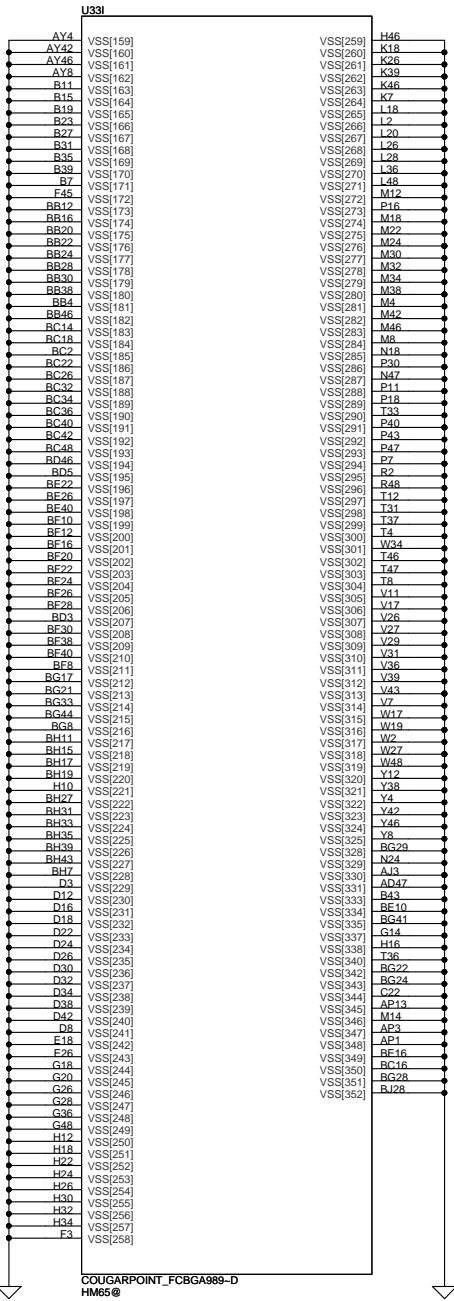
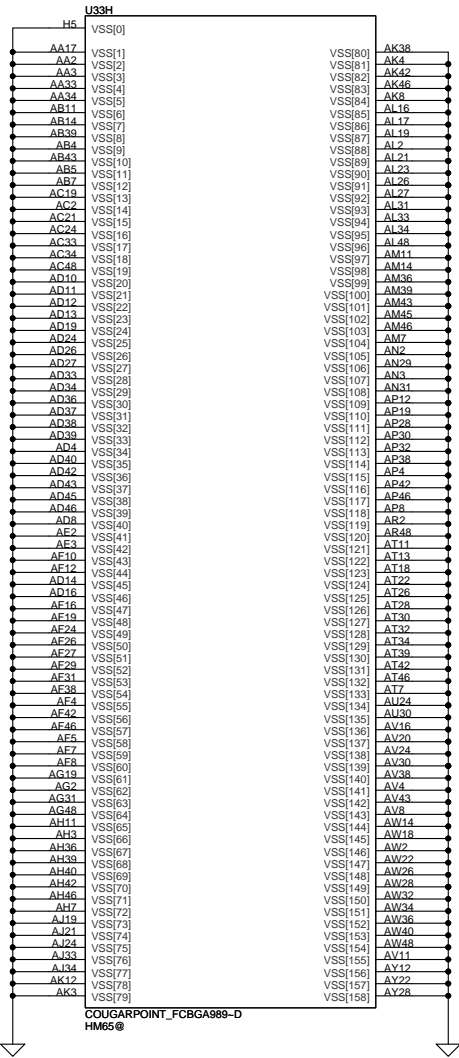
GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When used as SATA2GP/SATA3GP for mechanical presence detect
L-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check log page 47

```

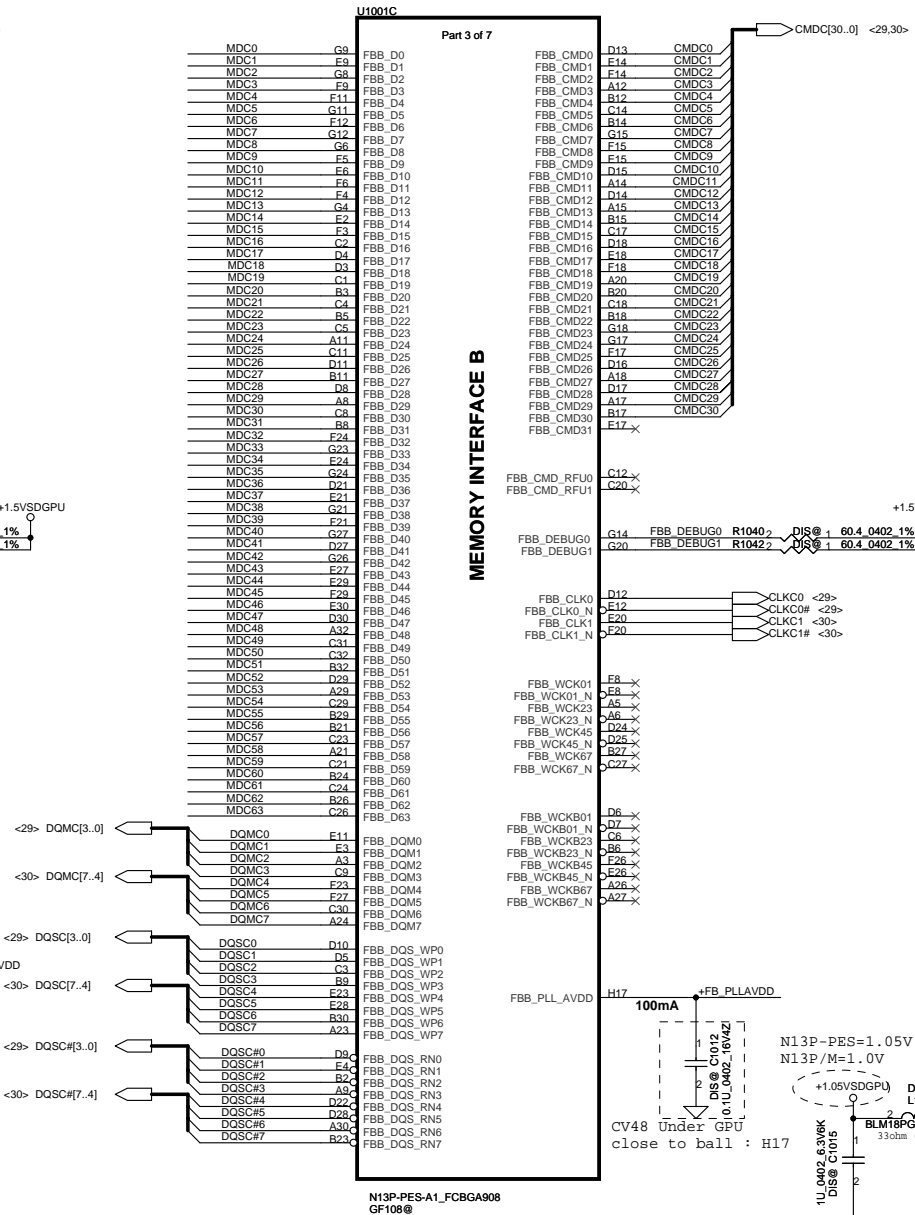
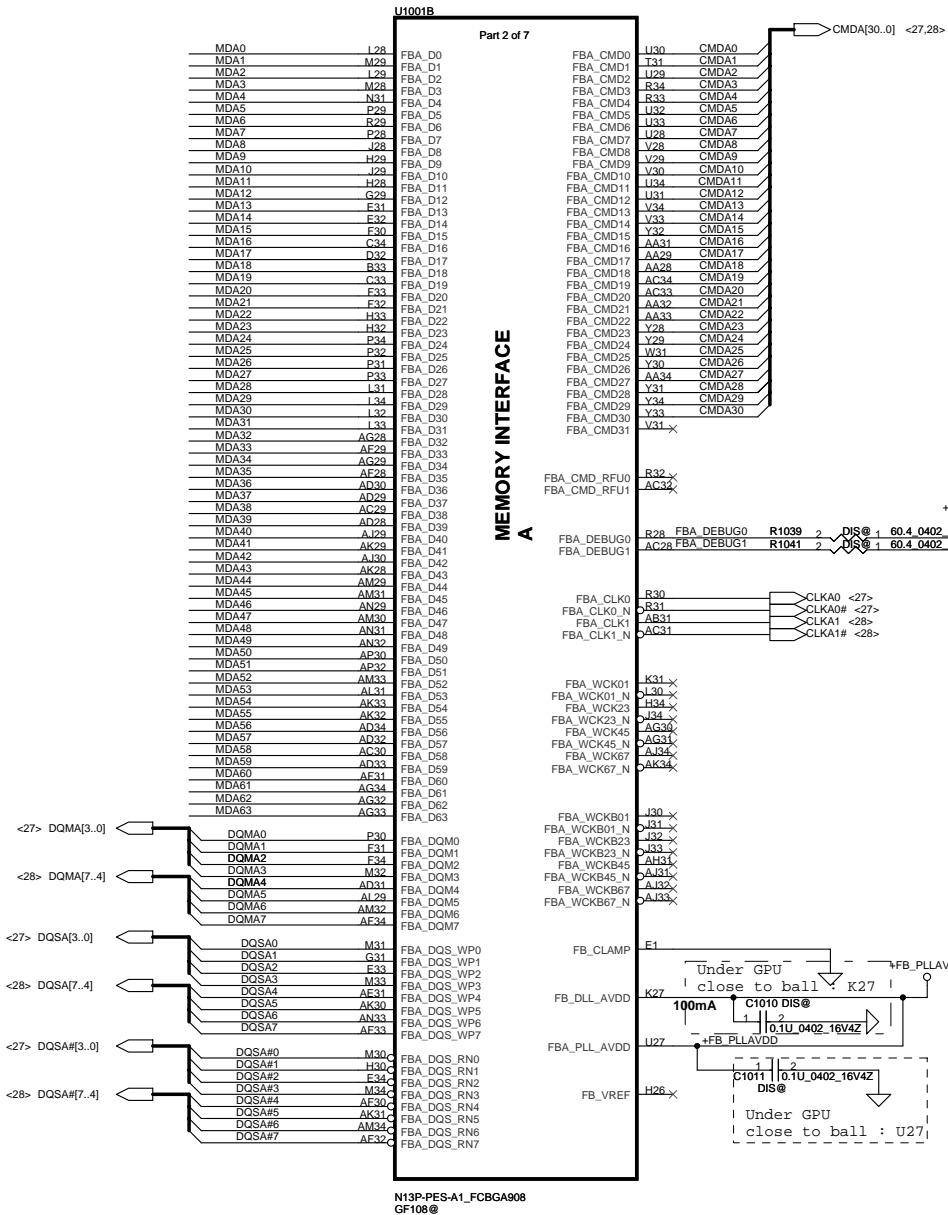
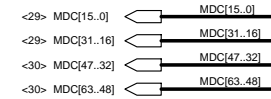
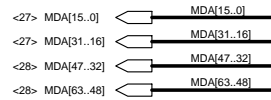


Project ID	GPIO69	GPIO7
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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Date:	Friday, January 06, 2012	Sheet	18 of	60	

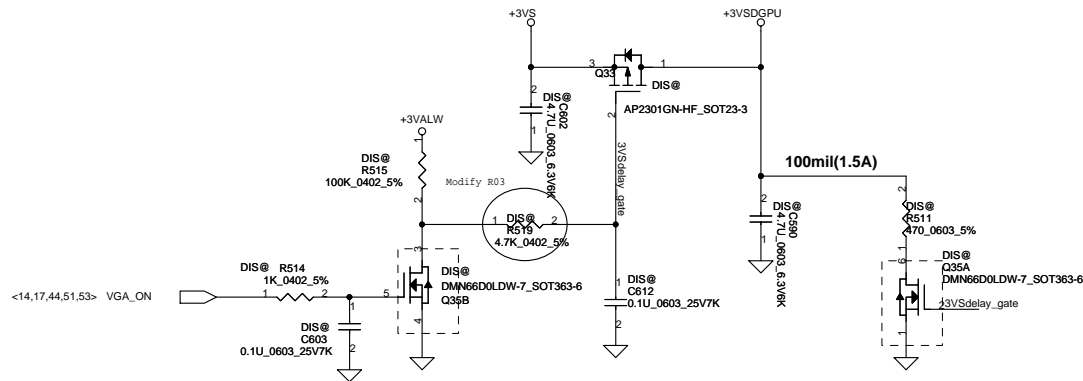


VRAM Interface

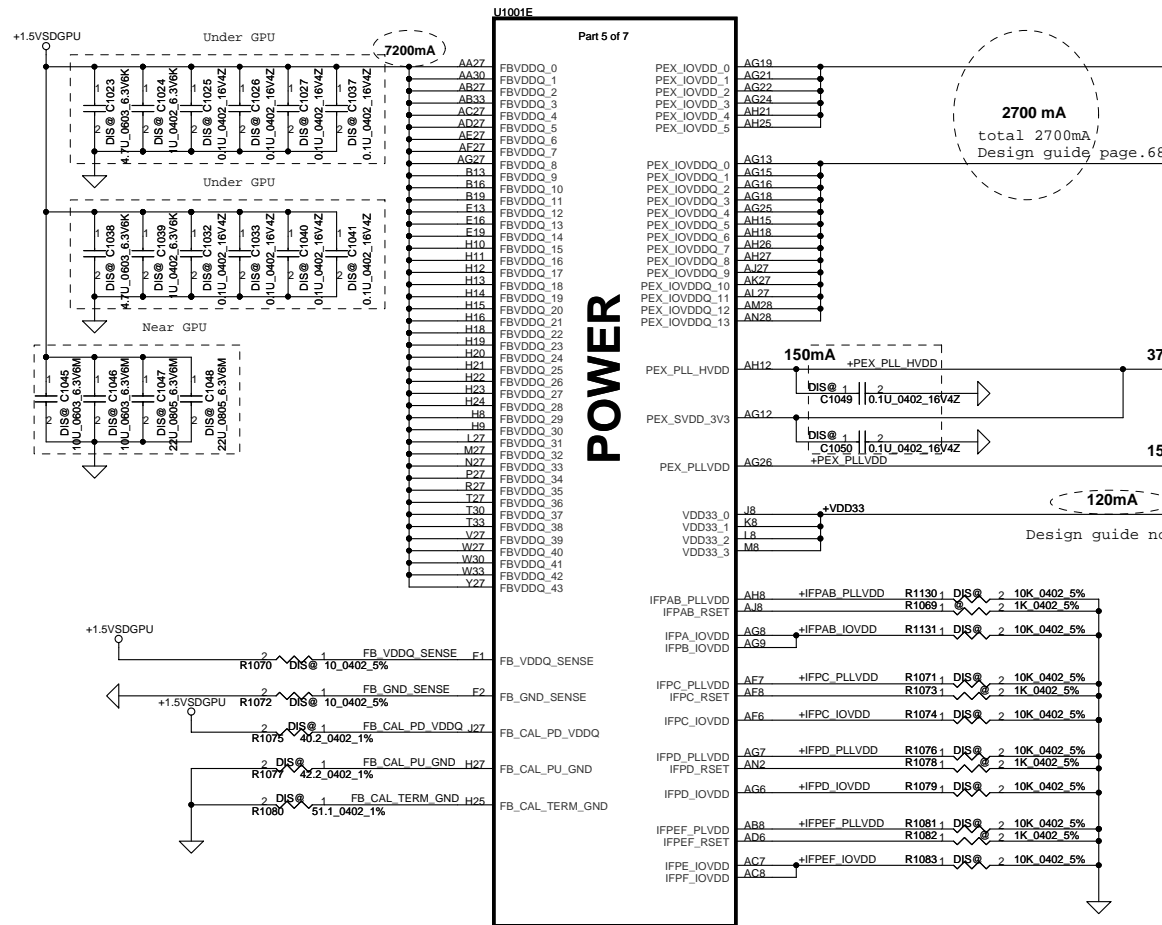


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				Customer	Document Number	Rev B
				Date:	40191D	
				Friday, January 06, 2012	Sheet 23 of (6)	

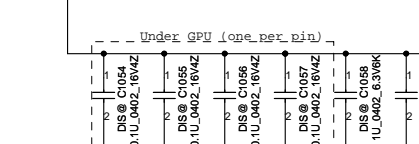
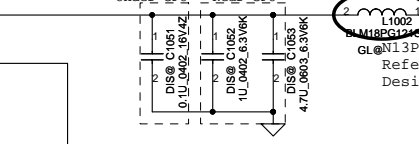
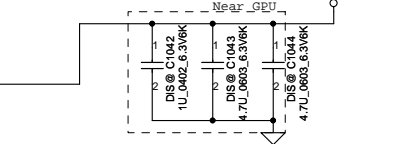
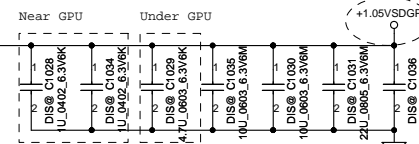
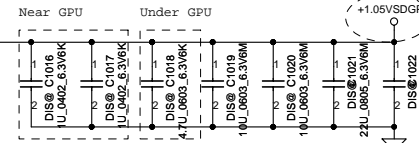
+3VS to +3VSDGPU for GPU



Design guide no define



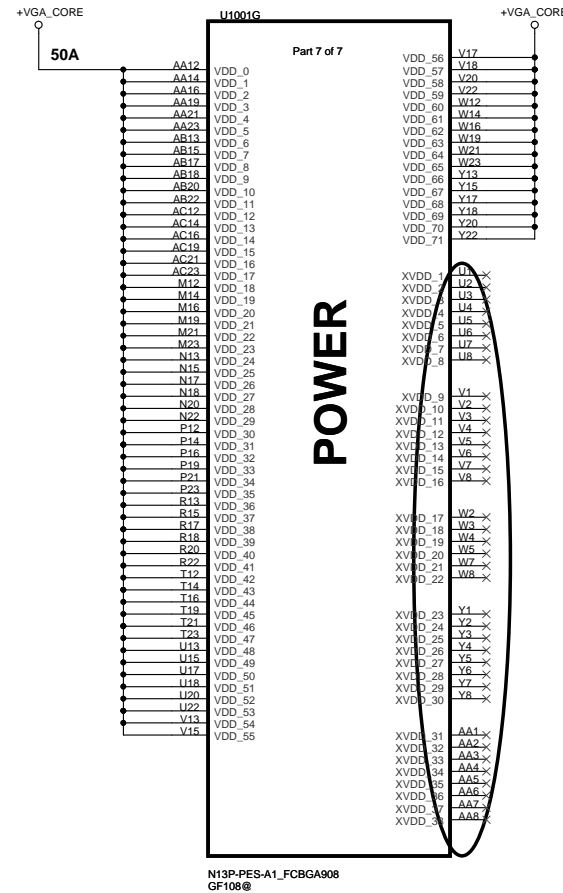
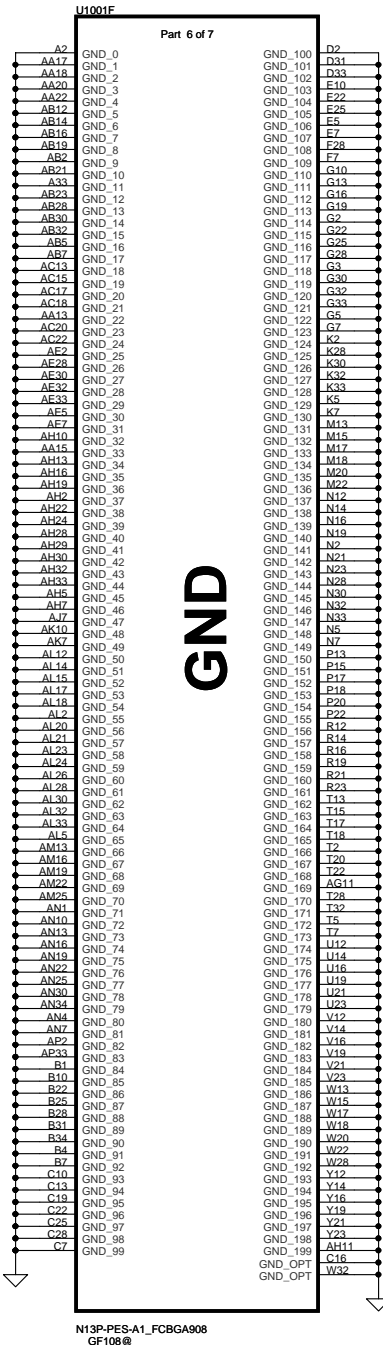
N13P-PPS-A1_FCBGA908
GF108@



Reference Sch = 300R@100MHz
Design Guide page69 未定義

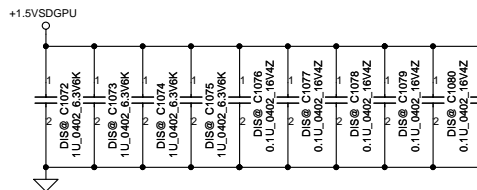
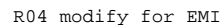
L1004	L1005
0.0603_5% GM@	0.0603_5% GS@
SD013000080	SD013000080

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						Date: Friday, January 06, 2012		Sheet 25 of 60			



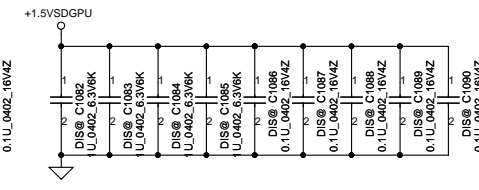
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								Rev		Document Number				Rev	
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Date:								Friday, January 06, 2012		Sheet		26 of 60			

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



oup1

Gro



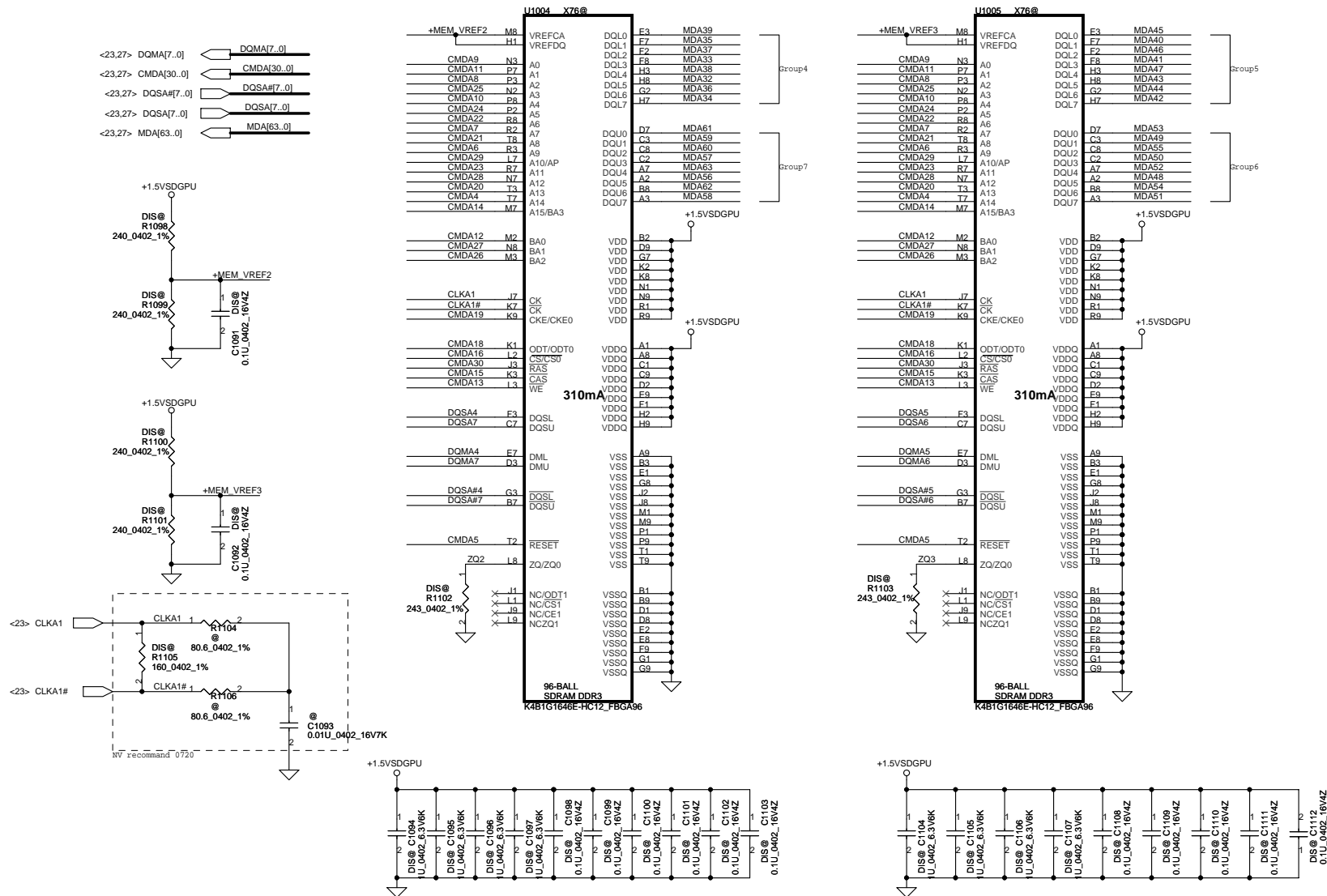
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DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Docu Custom	Document Number 40191D	Rev B
Date:				Friday, January 06, 2012		
				Sheet 27 of 61		

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



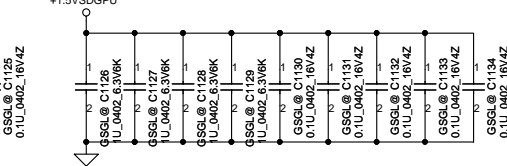
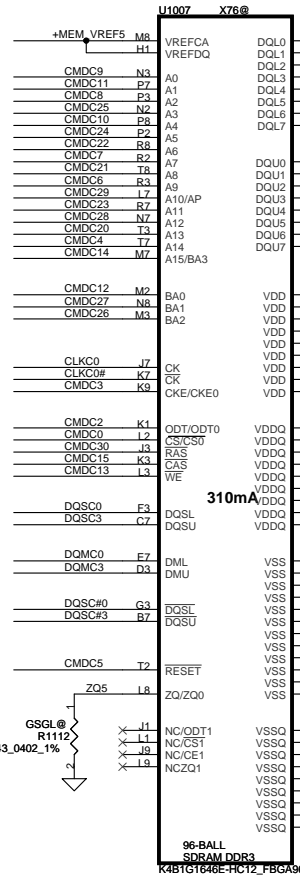
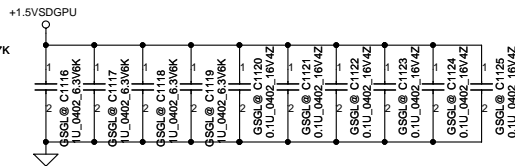
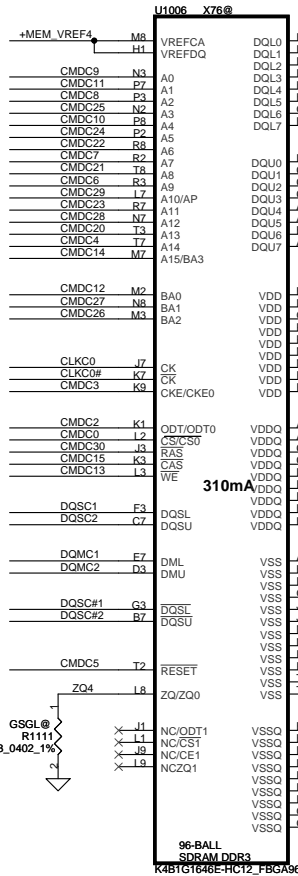
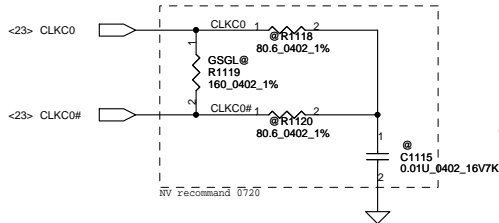
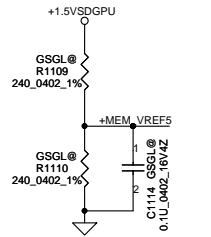
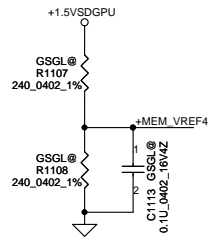
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
LOW		HIGH

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

<23,30> DQSC[7..0] DQSC[7..0]
<23,30> DQSC#[7..0] DQSC#[7..0]
<23,30> DQMC[7..0] DQMC[7..0]
<23,30> MDC[63..0] MDC[63..0]
<23,30> CMDC[30..0] CMDC[30..0]



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

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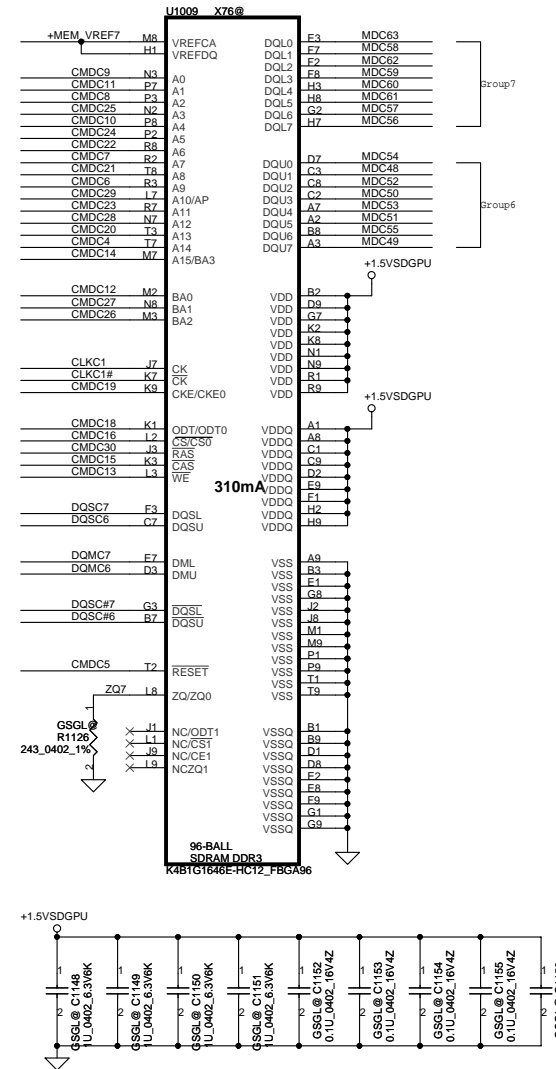
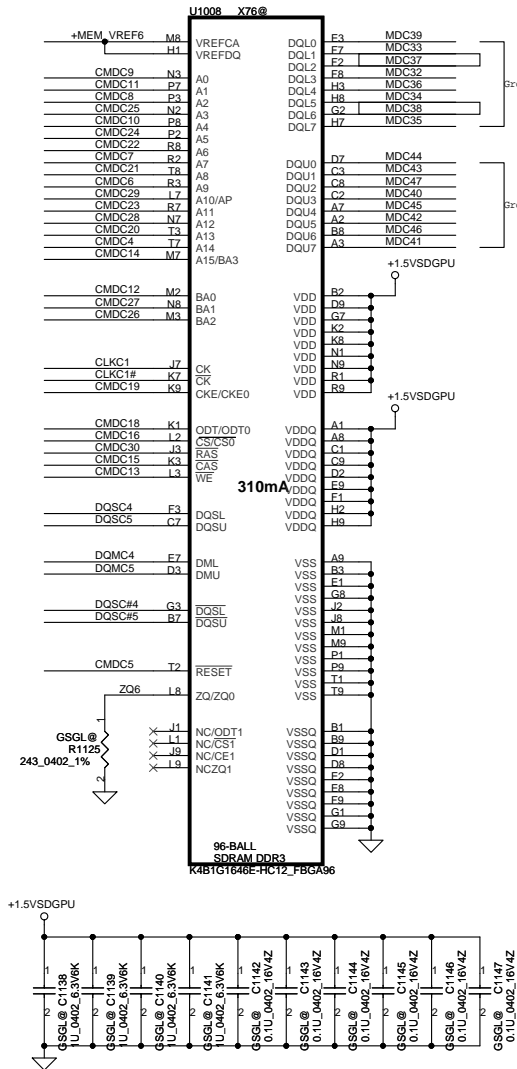
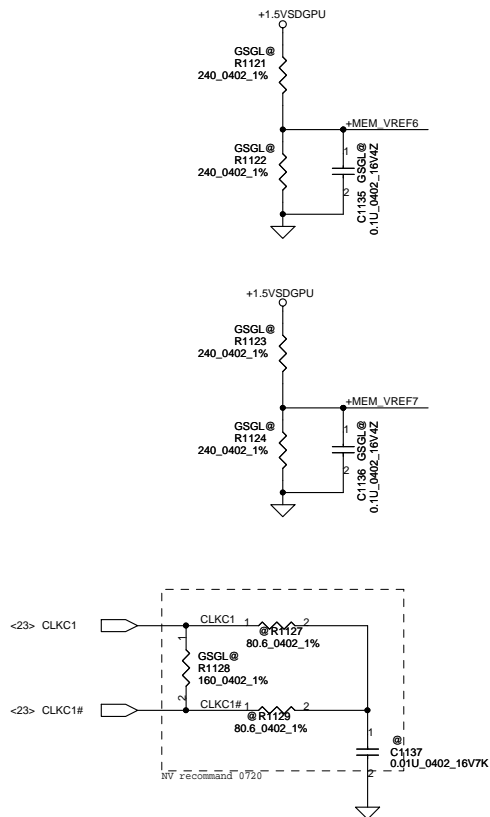
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

<23,29> DQMC[7..0] ← DQMC[7..0]
<23,29> CDMC[30..0] ← CDMC[30..0]
<23,29> DQSC# [7..0] ← DQSC# [7..0]
<23,29> DQSC[7..0] ← DQSC[7..0]
<23,29> MDC[63..0] ← MDC[63..0]

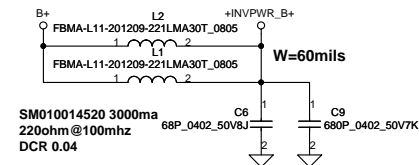
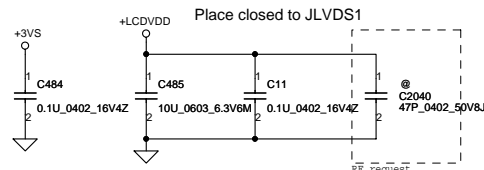
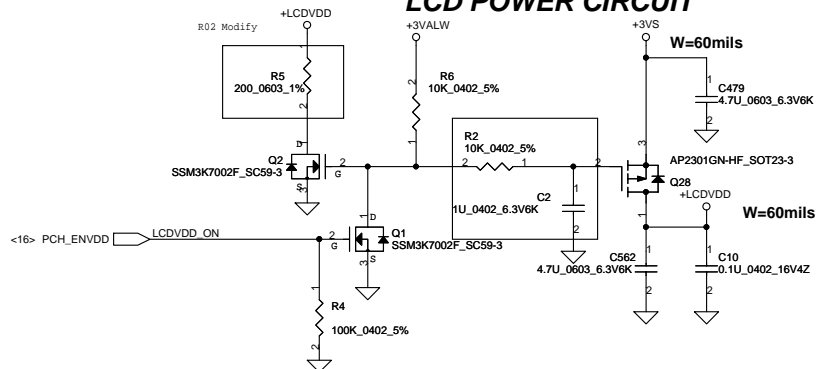
R02 modify
Swap MDC37 and MDC38



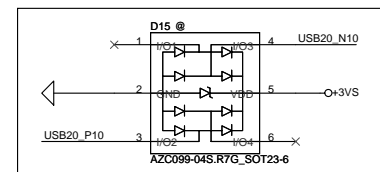
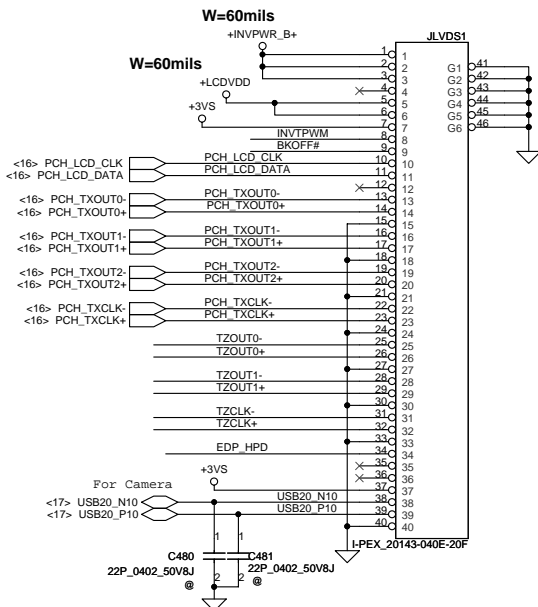
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

LCD POWER CIRCUIT

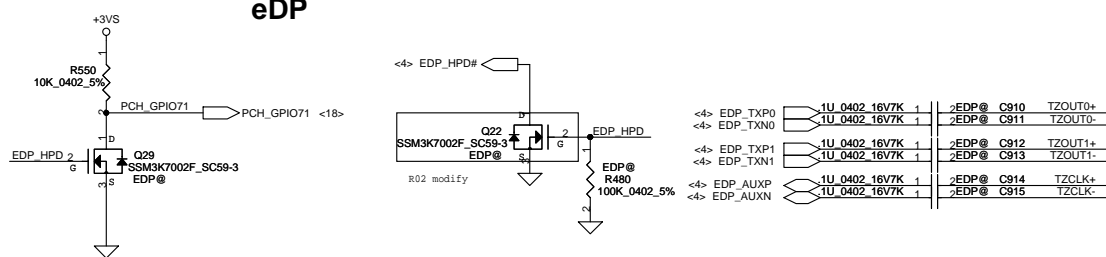


LCD/LED PANEL Conn.



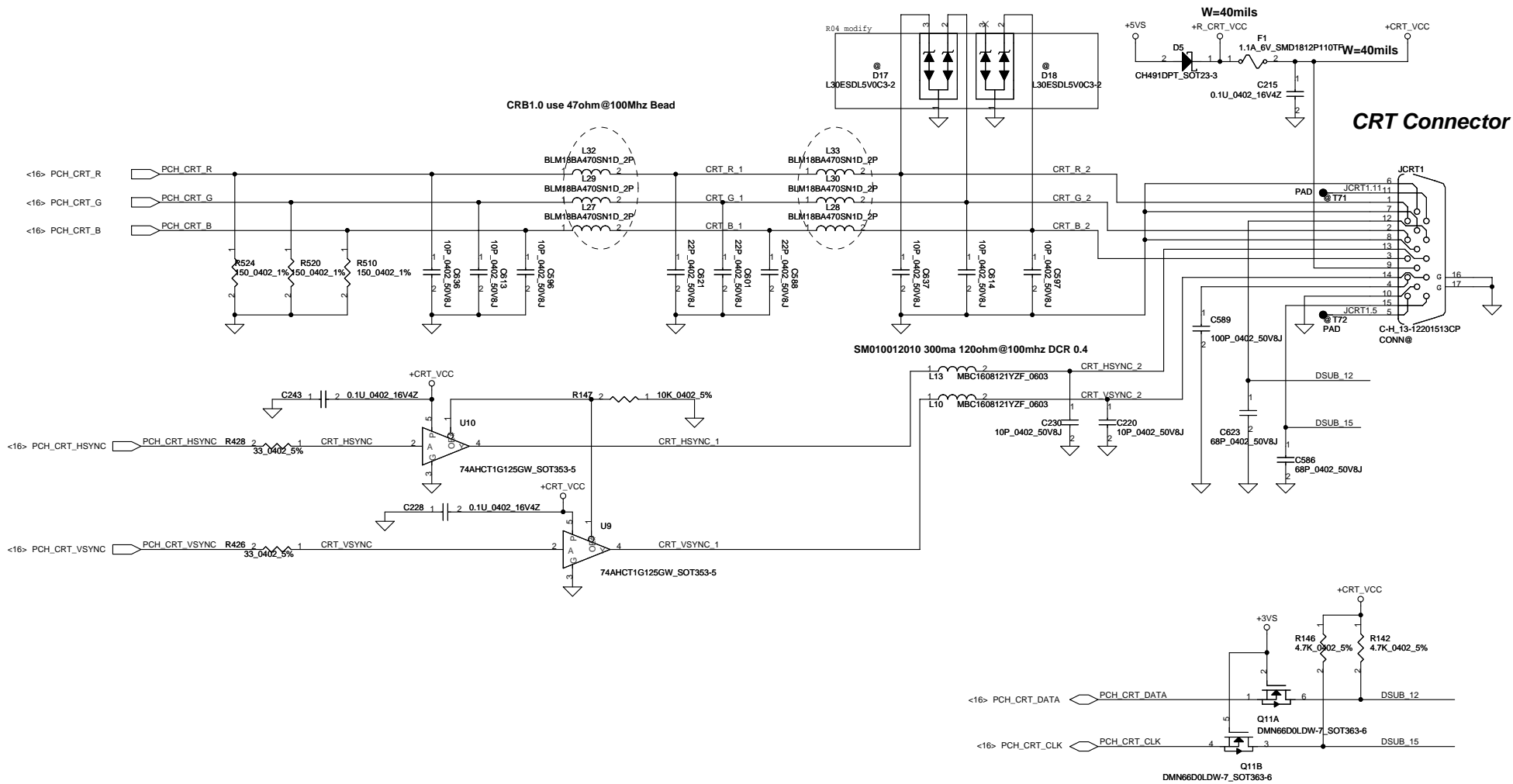
Modify R02

eDP

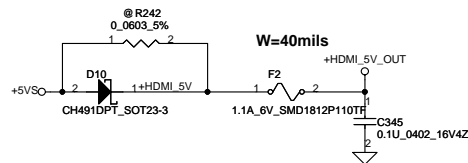


	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1

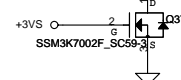
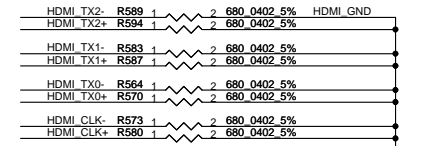
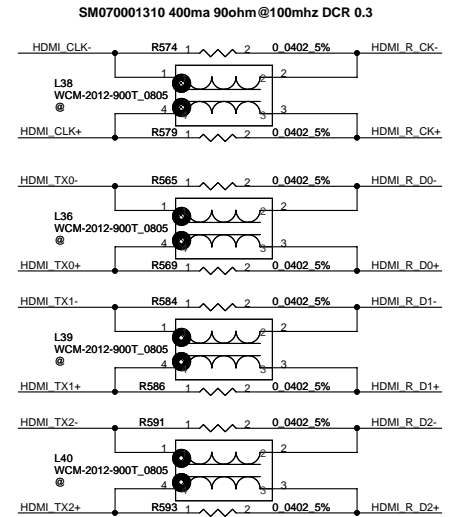
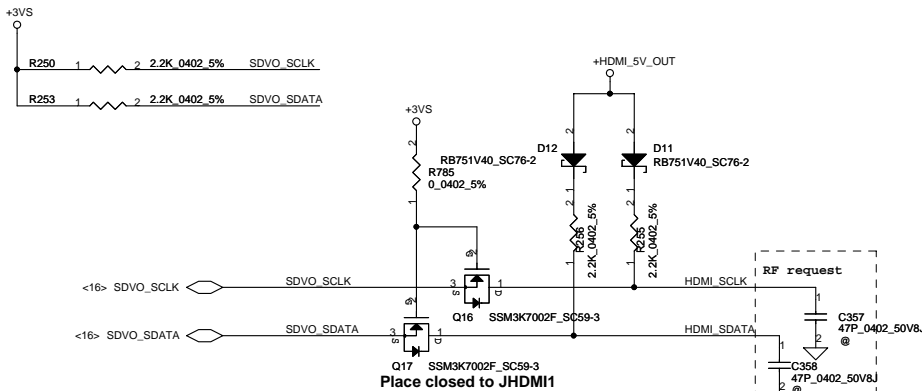
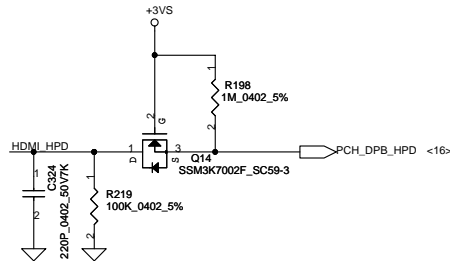
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				Date:	Friday, January 06, 2012
				Sheet	31 of 60
				Rev	B



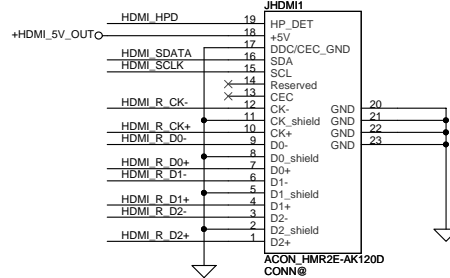
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				Date	Friday, January 06, 2012
				Sheet	32 of 60



<16> PCH_DPB_N0	C280	2	1	.1U_0402_16V7K	HDMI TX2-
<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+

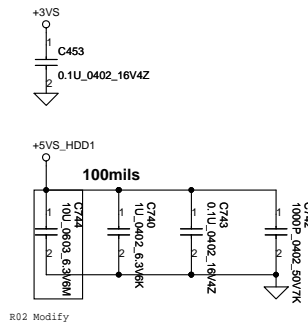
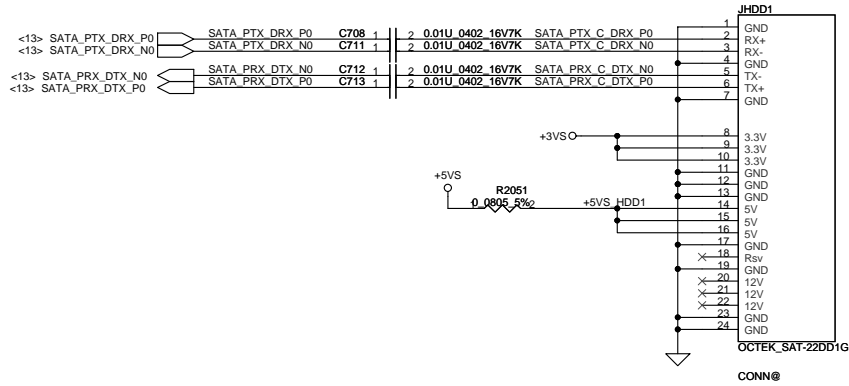


HDMI connector



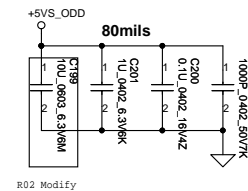
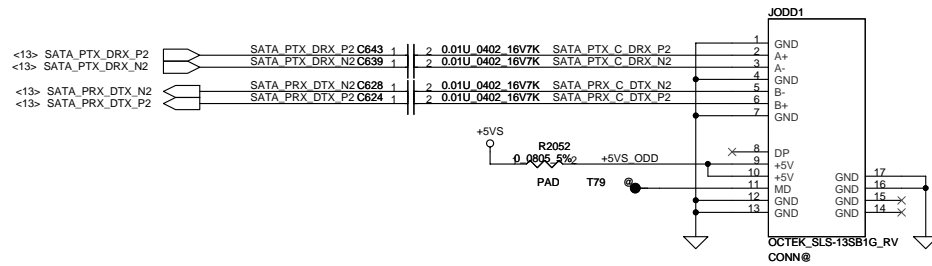
SATA HDD1 Conn.

CL 4.0 mm



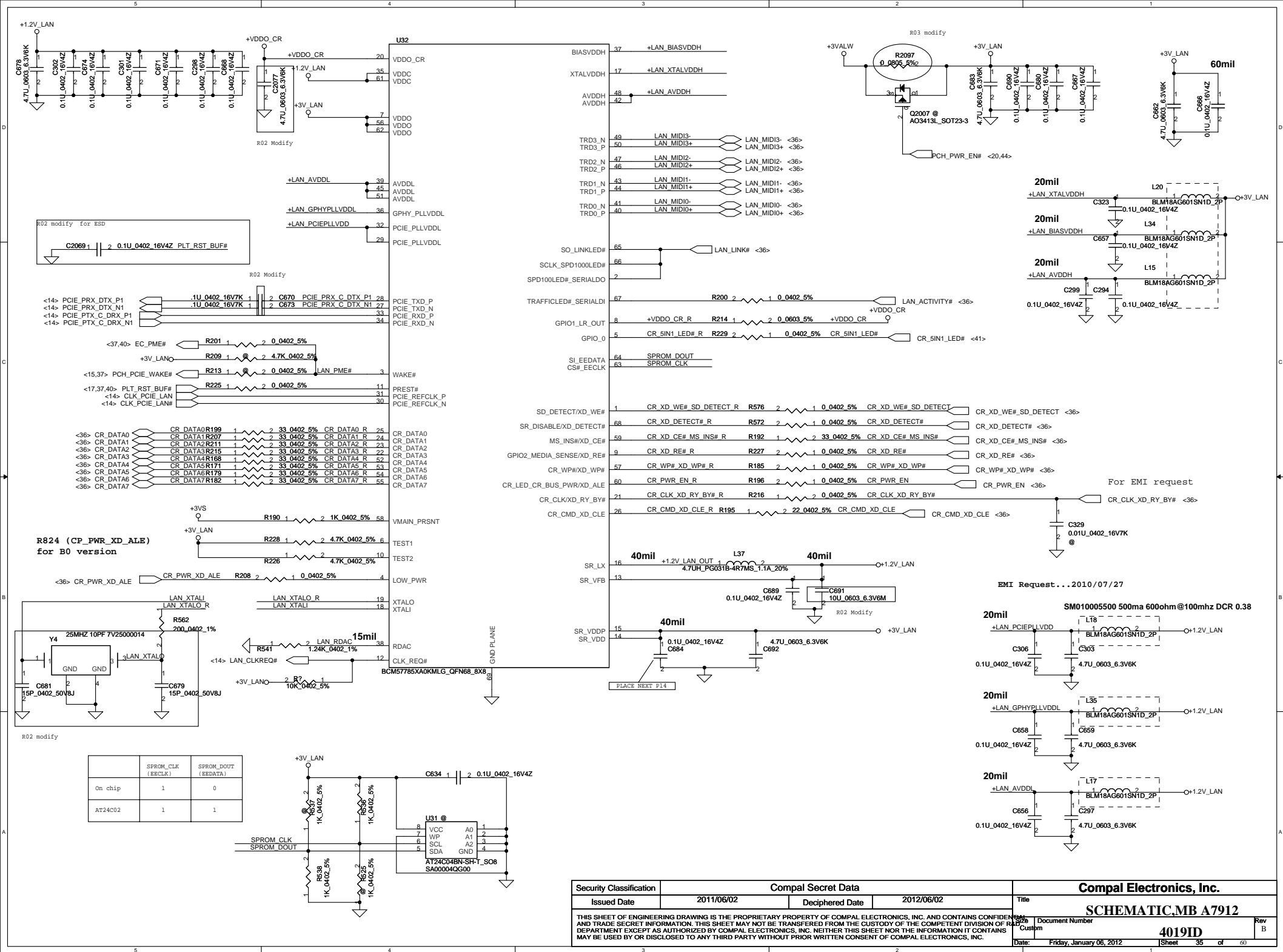
R02 Modify

SATA ODD Conn.

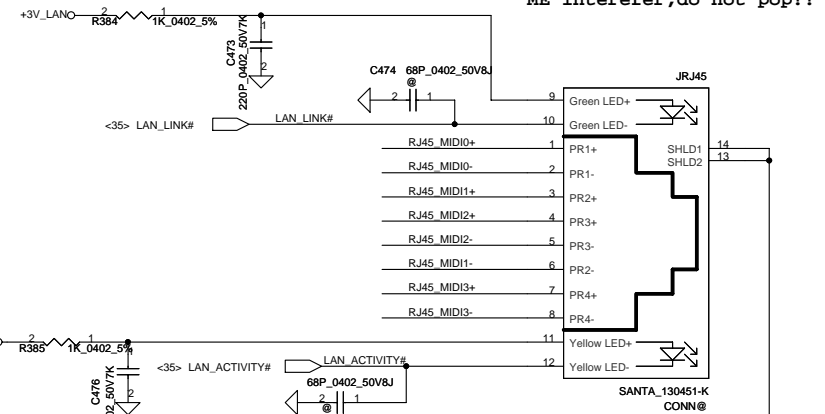


R02 Modify

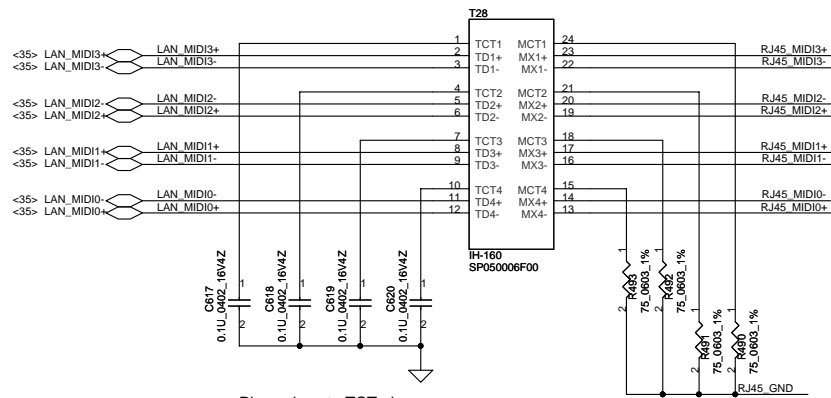
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Issued Date				2011/06/02				Deciphered Date			
2012/06/02				Title				Schematic, MB A7912			
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Date: Friday, January 06, 2012				Rev				B			
1				Sheet				34 of 60			



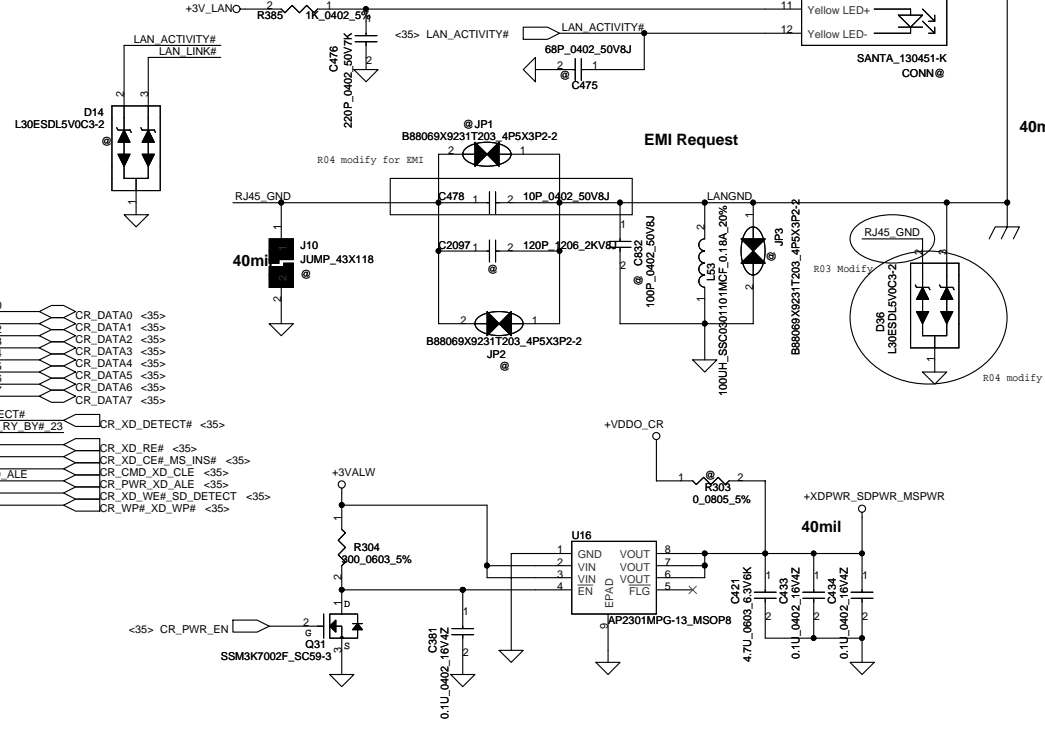
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				Custom	B
Date:	Friday, January 06, 2012	Sheet	35	of	60



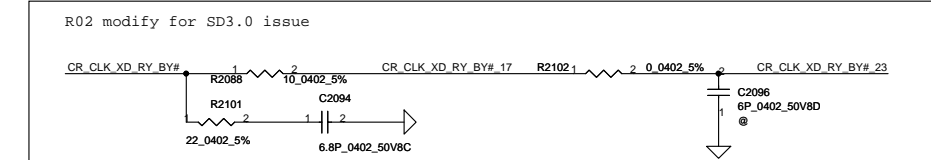
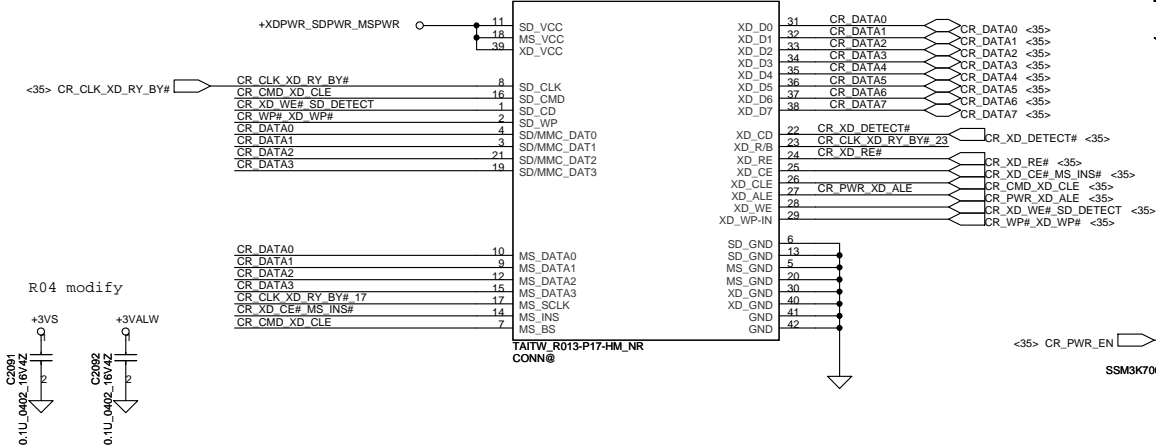
40mil



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

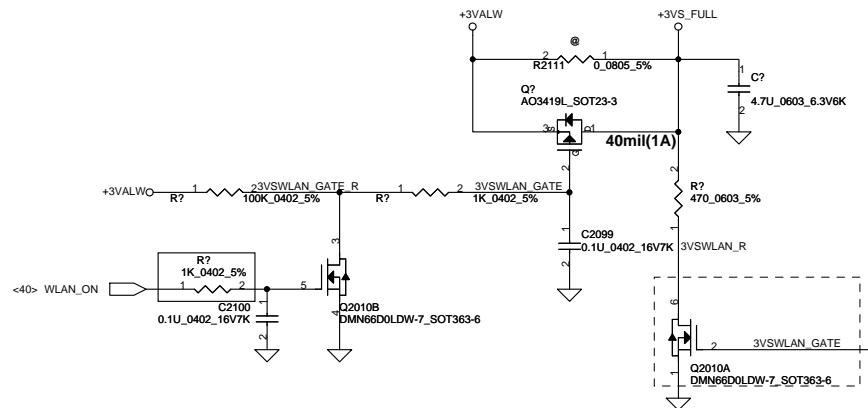
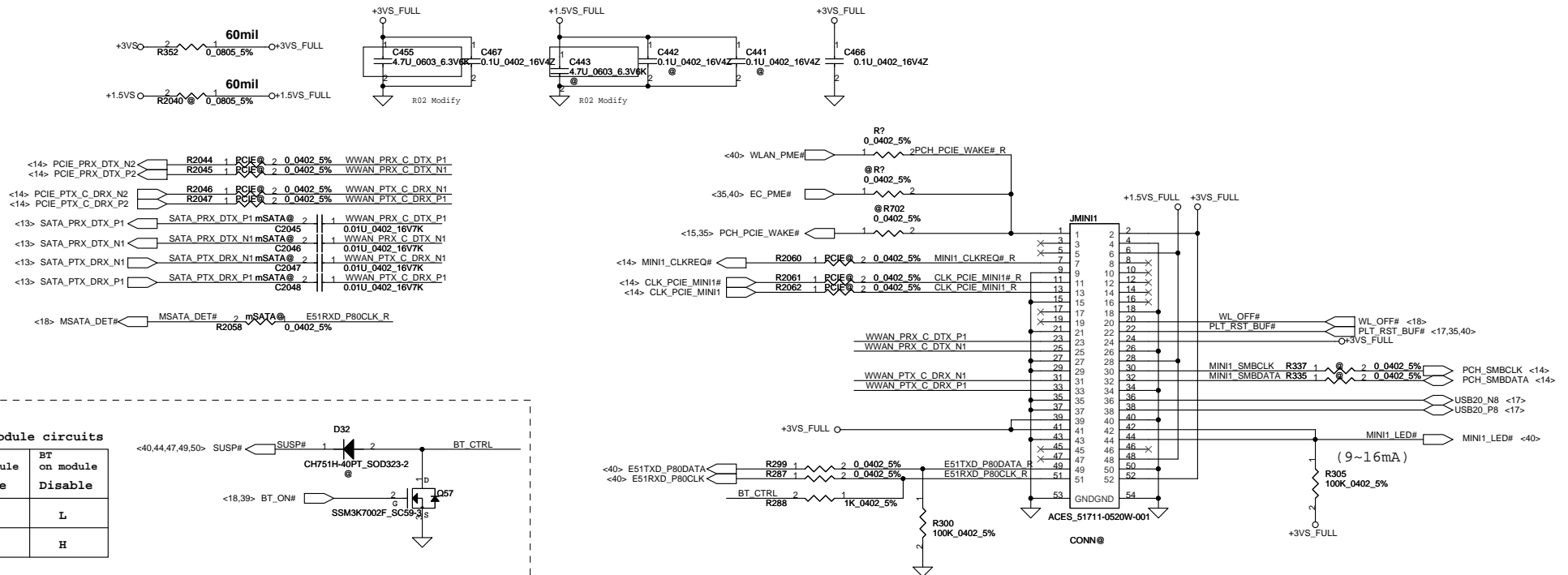


TAITW_R013-P17-HM_NR
CONN@

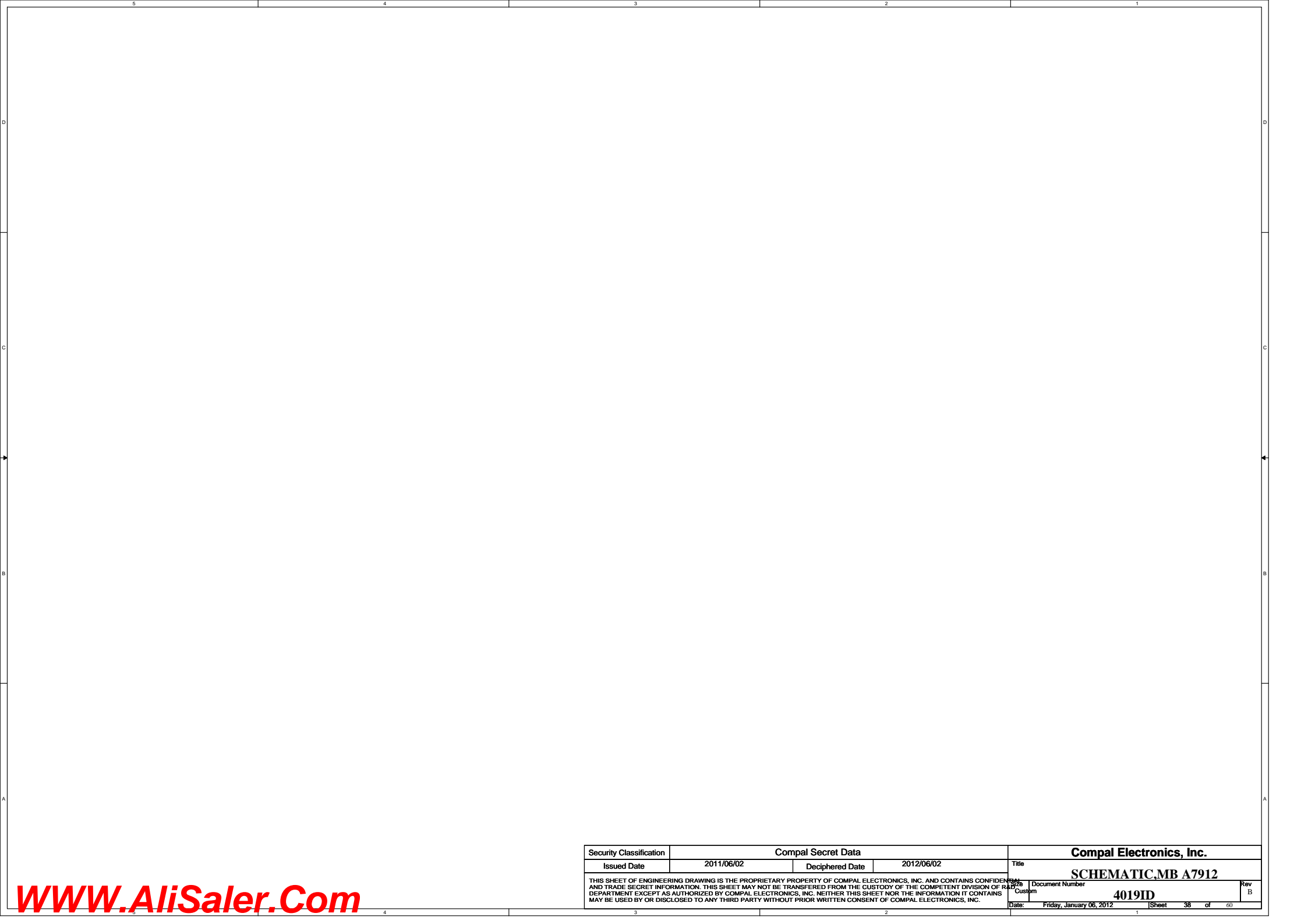


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				Custom	4019ID	
Date: Friday, January 06, 2012				Sheet 36 of 60		

For Wireless LAN or MSATA



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				Document Number Custom	40191D
Date:				Friday, January 06, 2012	Sheet 37 of 61



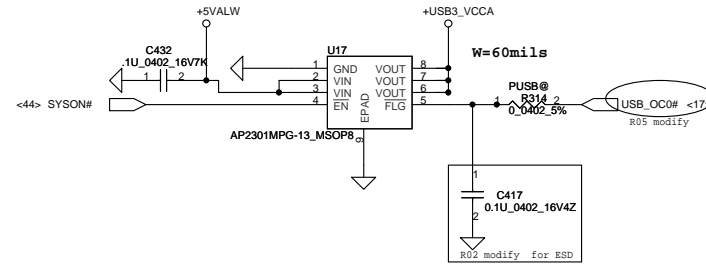
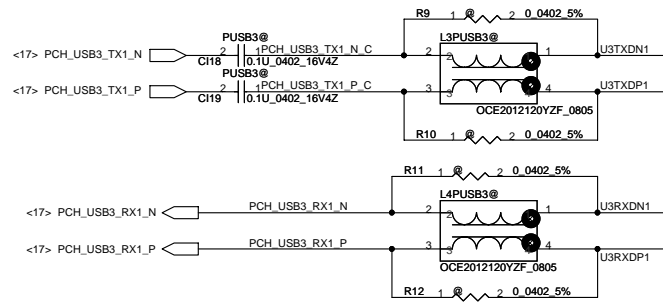
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				Document Number	4019ID
				Date: Friday, January 06, 2012	Sheet 38 of 60

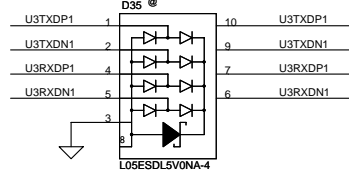
Deafult use PCH side USB3.0 signal

For USB2.0 ESD request

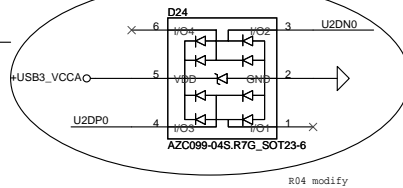
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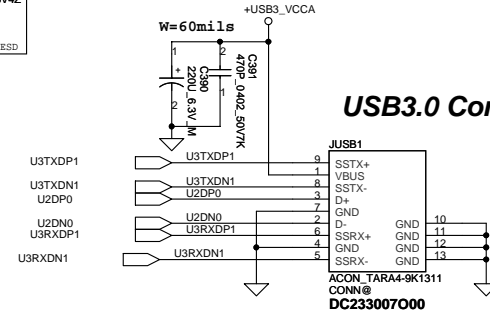
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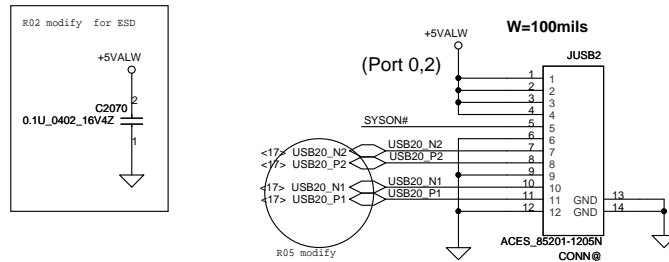
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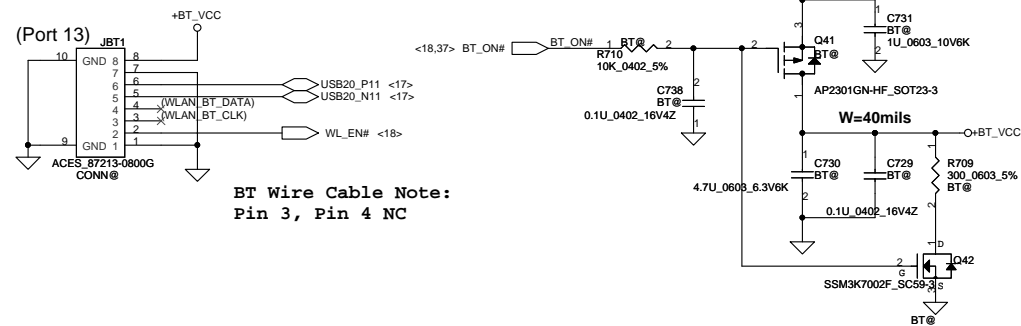
USB3.0 Conn.



USB/B Conn.



BT Conn.



BT Wire Cable Note:
Pin 3, Pin 4 NC

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				Date:	Friday, January 06, 2012	Sheet 39 of 60

Test Only
Bottom Side

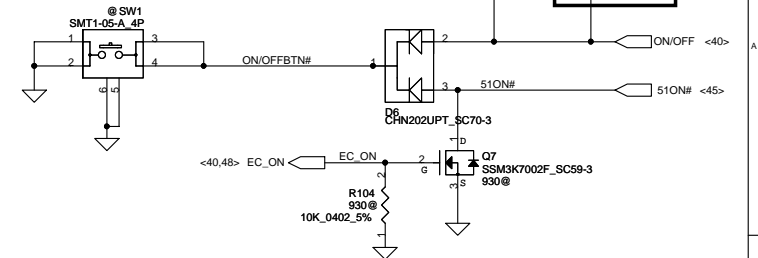
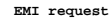


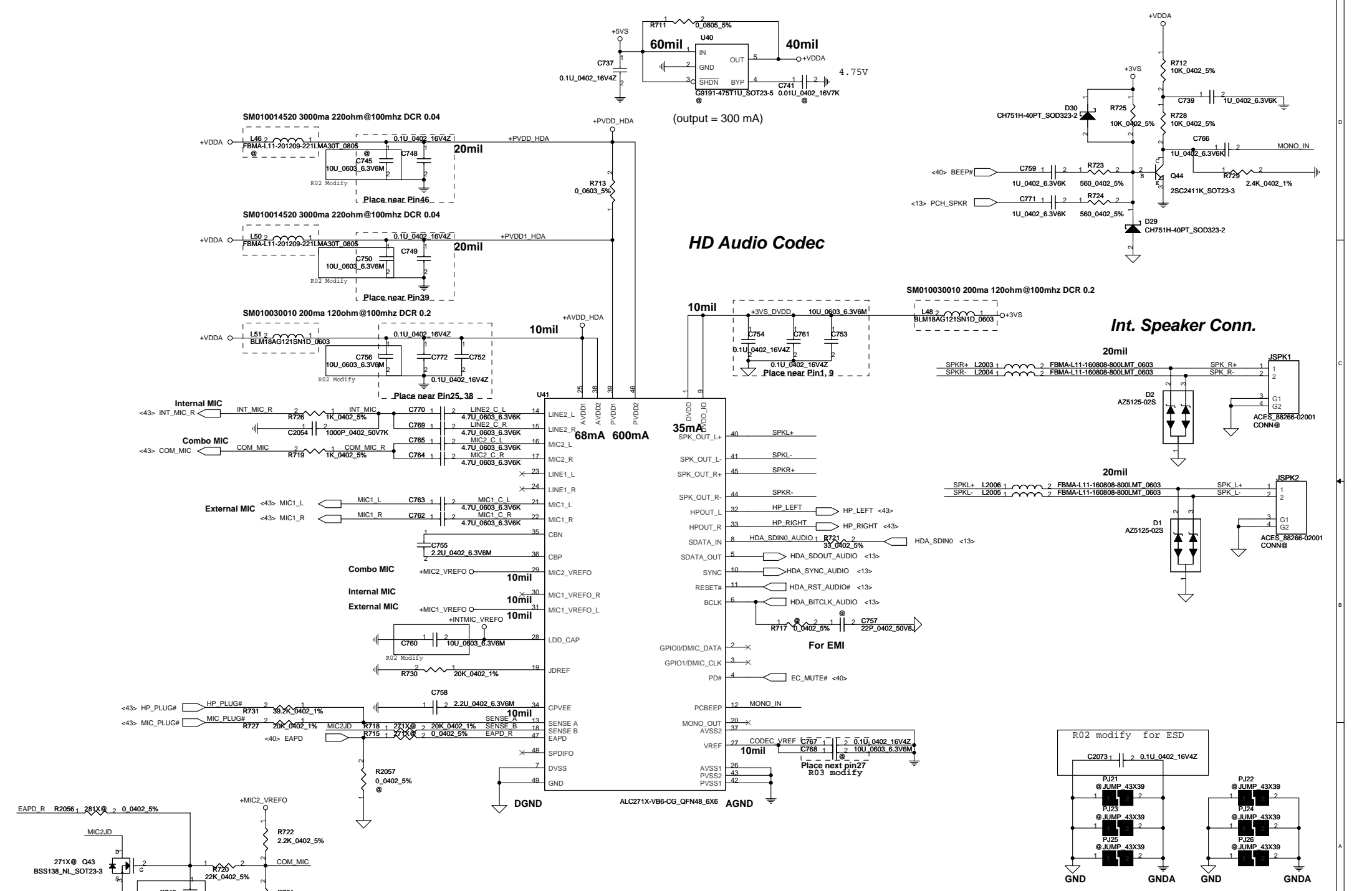
Diagram showing the connection for JPWR1 (Pin 1 to 10):

- Pin 1: LID_SW# (Signal)
- Pin 2: LID_SW# (Signal)
- Pin 3: LID_SW# (Signal)
- Pin 4: LID_SW# (Signal)
- Pin 5: PWR_LED# (Signal)
- Pin 6: ON/OFFBTN# (Signal)
- Pin 7: ON/OFFBTN# (Signal)
- Pin 8: ON/OFFBTN# (Signal)
- Pin 9: GND
- Pin 10: GND

Additional labels: +3V1W, LID_SW# <40>, +3VS.

The schematic diagram illustrates the TP Conn. circuit. It features a JTP1 connector with pins 1 through 10. Pin 1 is connected to D_CK_SCLK, and pin 2 is connected to TP_VDD. Pins 3 and 4 are connected to LEFT_BTN# and RIGHT_BTN# respectively. Pin 5 is connected to D_CK_SDATA, and pin 6 is connected to TP_CLK. Pins 7 and 8 are connected to TP_DATA and TP_DATA respectively. Pins 9 and 10 are connected to GND. The circuit includes several capacitors: C2101 (56P_0402_50V8K), C2102 (56P_0402_50V8K), C2103 (56P_0402_50V8K), C2104 (56P_0402_50V8K), C2105 (56P_0402_50V8K), C2106 (56P_0402_50V8K), and C2107 (56P_0402_50V8K). It also includes two switches, SW2 and SW3, both labeled SMT1-05-A 4P. A note indicates 'R04 modify' and 'Delete SW5, SW6'.

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				Custom	4019ID
Date: Friday, January 06, 2012				Sheet	41 of (6)



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					4019ID	Customer	
Date:		Friday, January 06, 2012		Sheet	42	of	(60)

Singatron 2SJ2326
DC021007151

Headphone Out

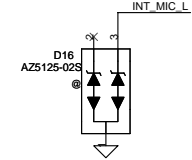
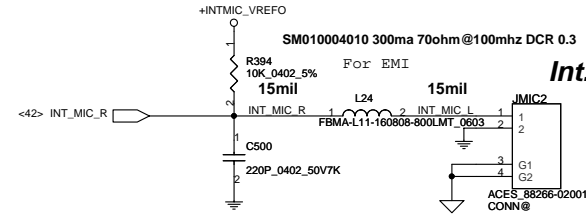
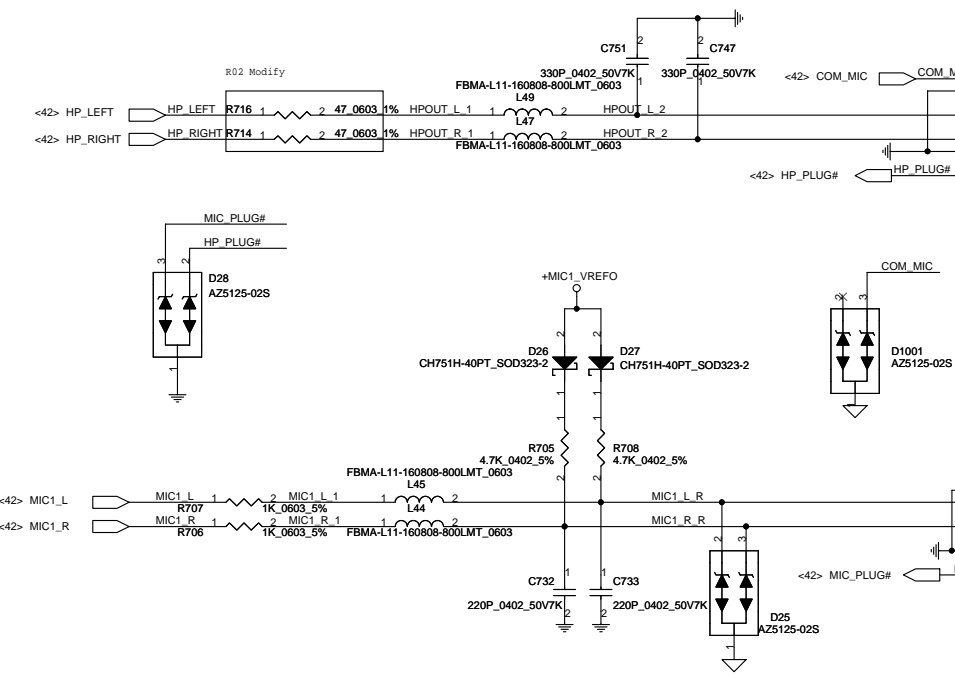
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CONN@

MIC JACK

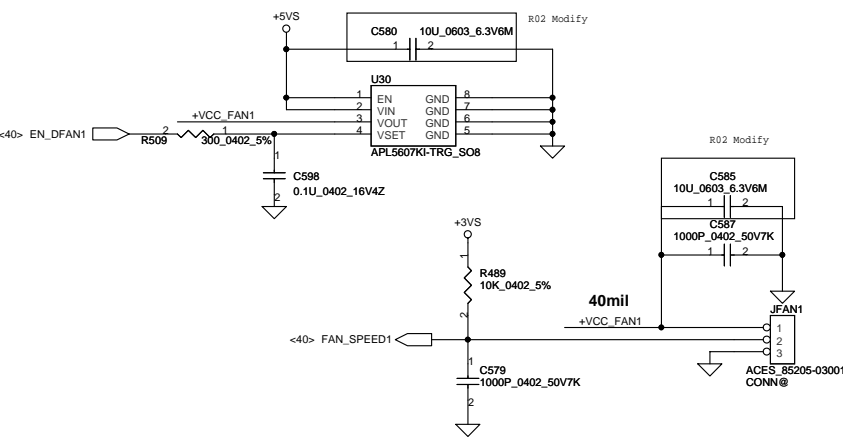
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Int. MIC

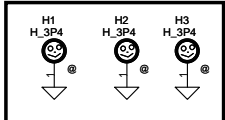
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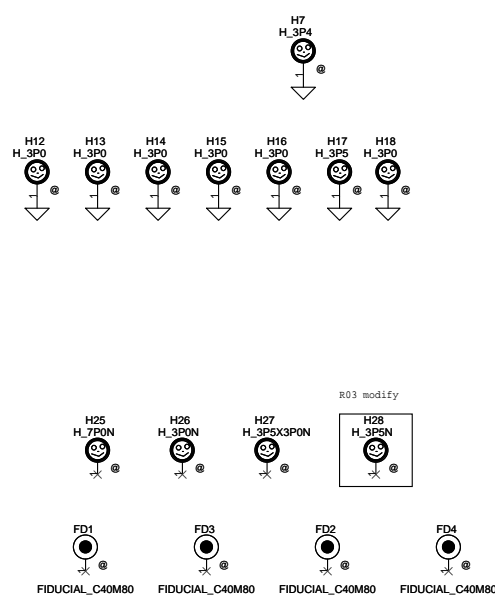
FAN1 Conn



FAN Stand-Off

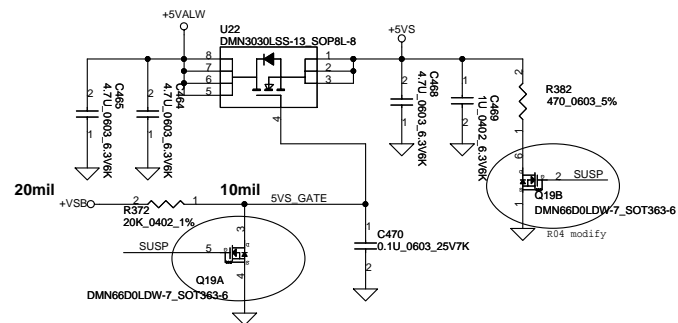


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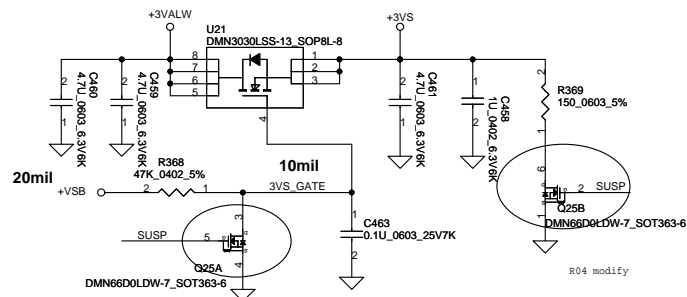


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Date: Friday, January 06, 2012				Sheet	43 of 60

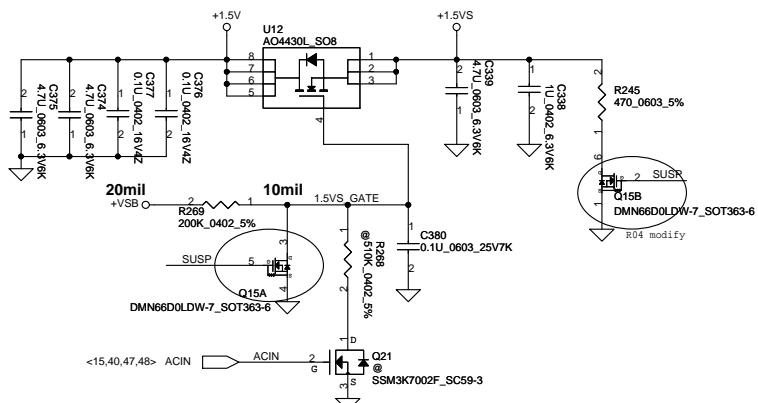
+5VALW TO +5VS



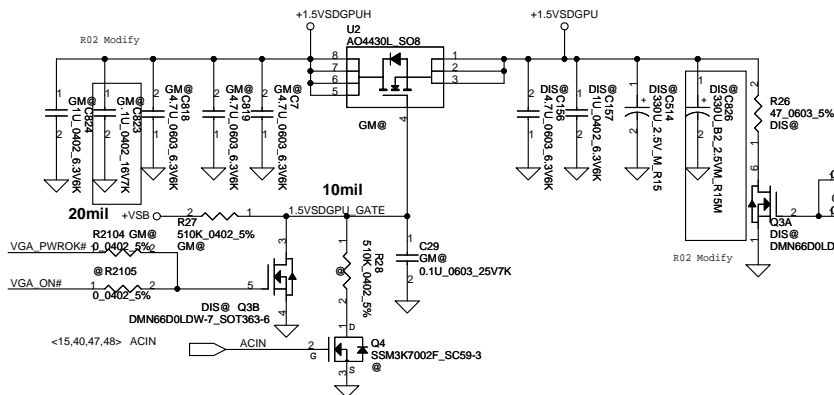
+3VALW TO +3VS

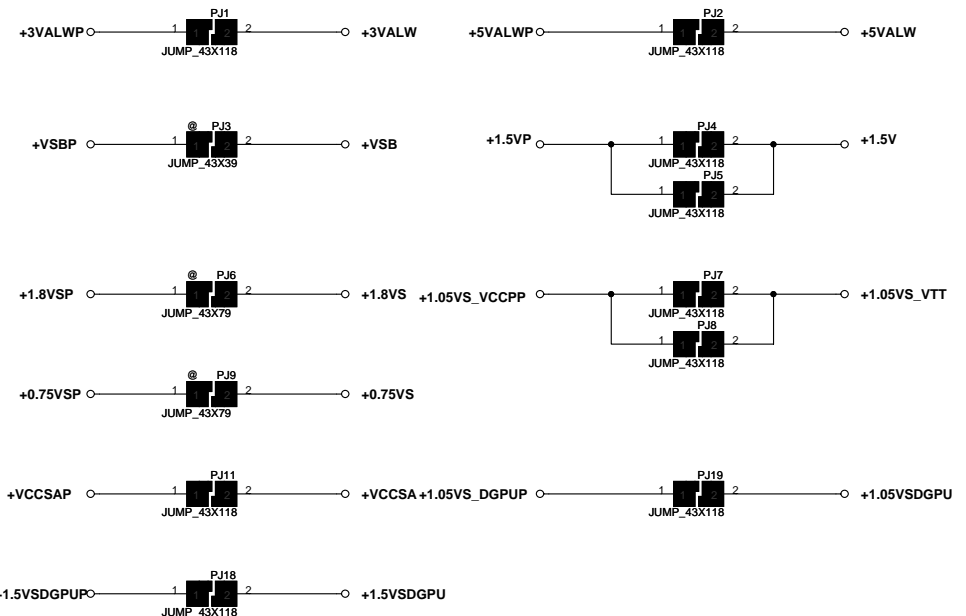
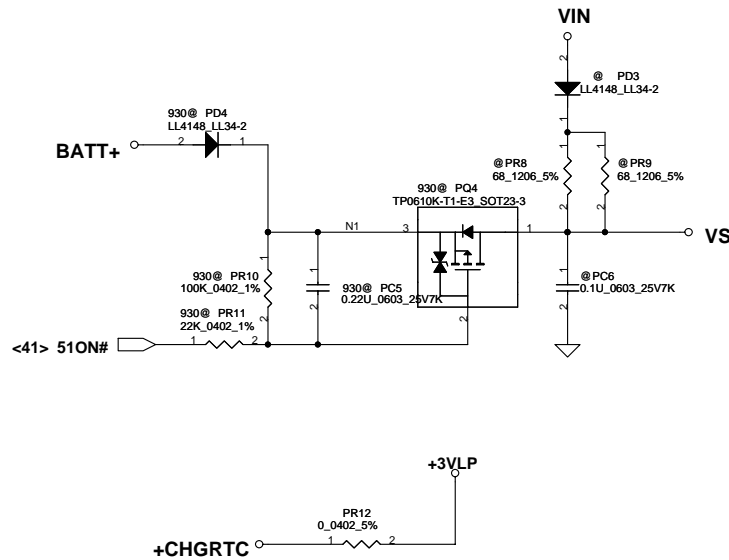
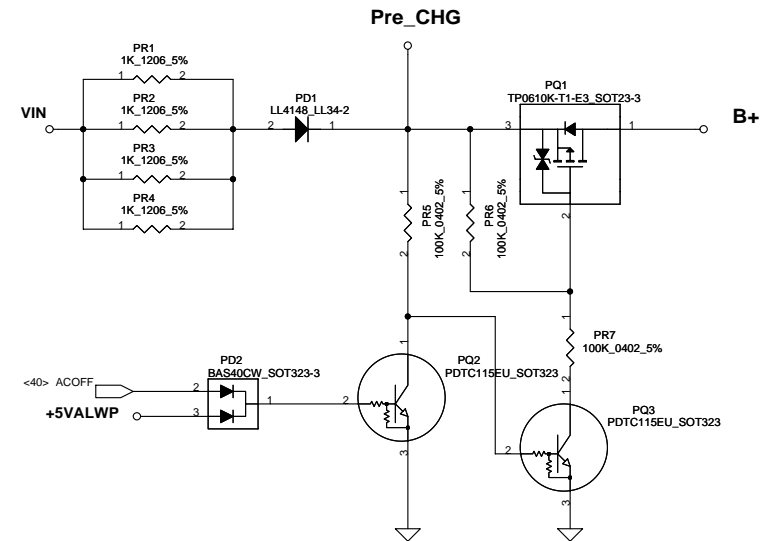
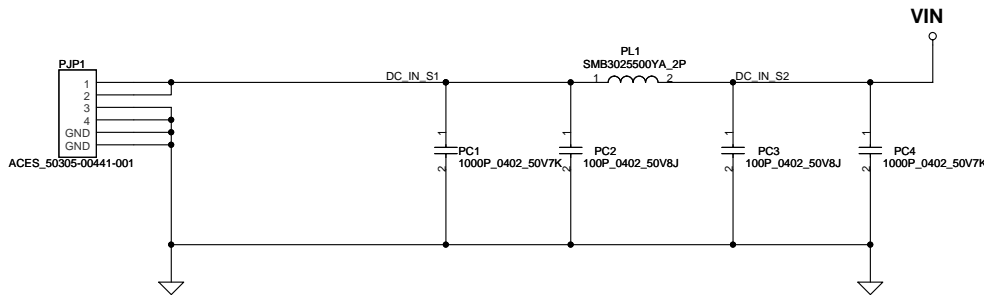


+1.5V to +1.5VS

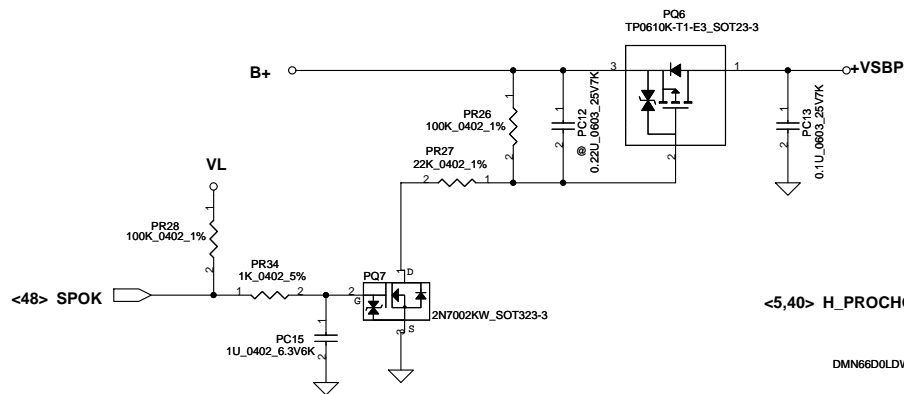
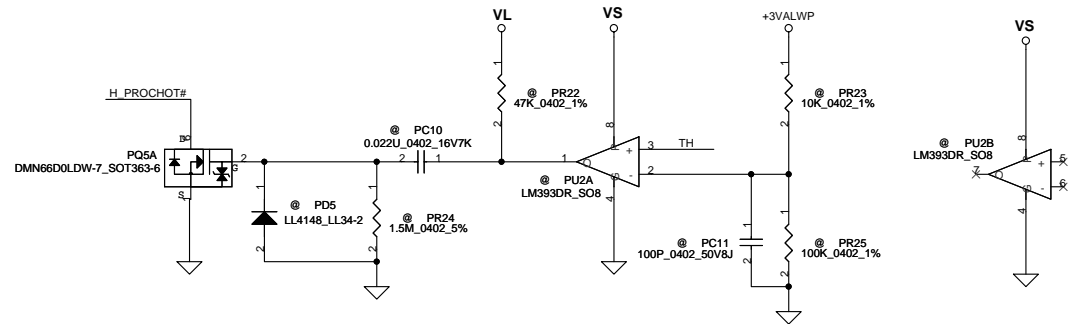
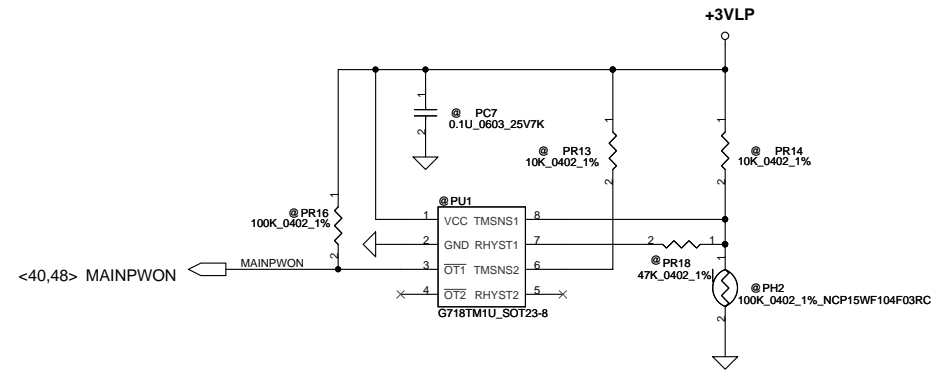
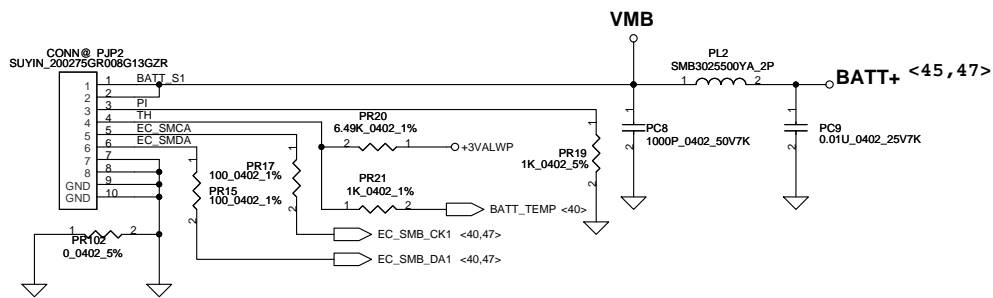


+1.5VSDGPUH to +1.5VSDGPU for GPU

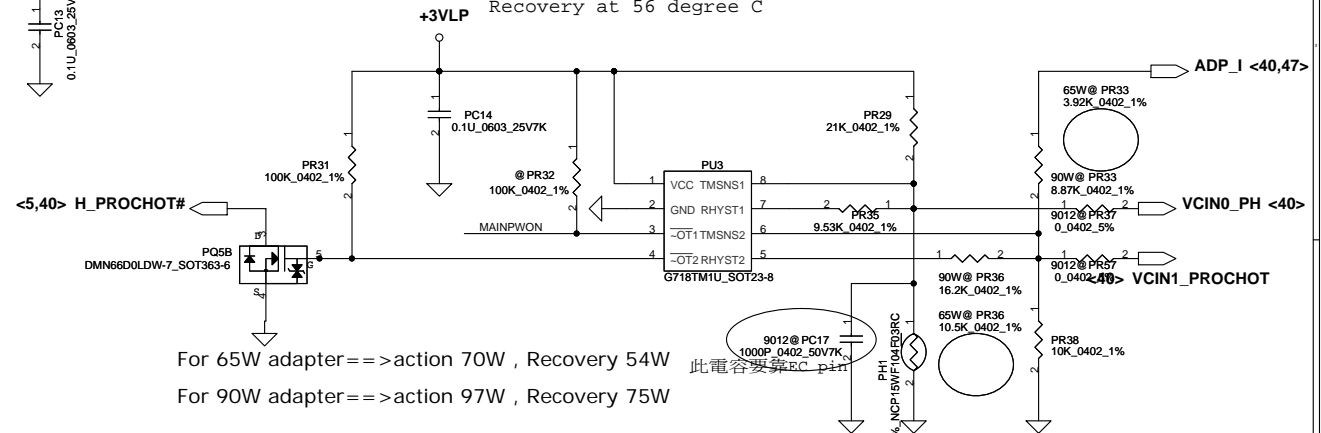




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				Date	Friday, January 06, 2012
				Sheet	45 of 60
				Rev	B



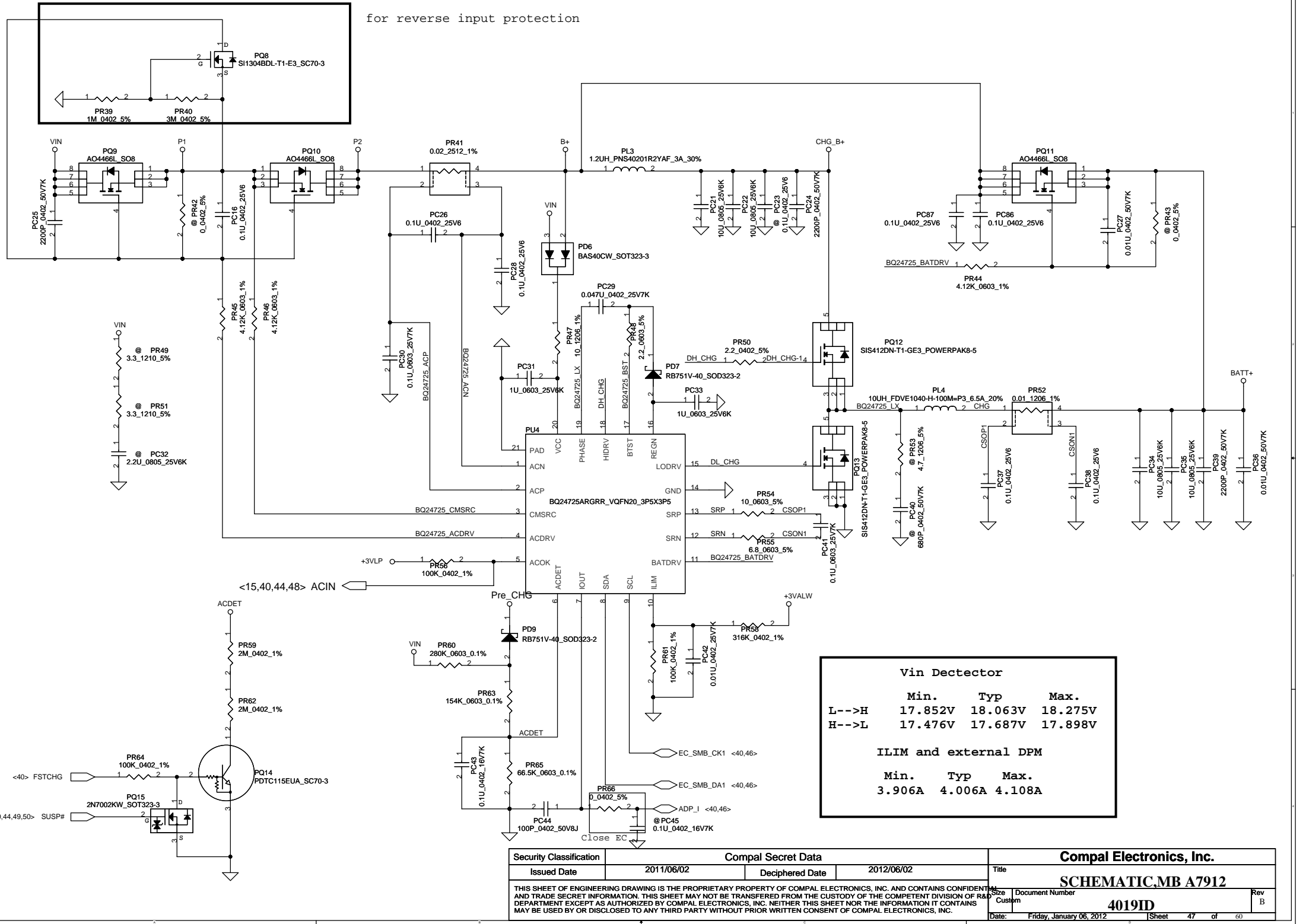
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W

此電容要算PC pin

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				Date	Friday, January 06, 2012
				Sheet	46 of 60

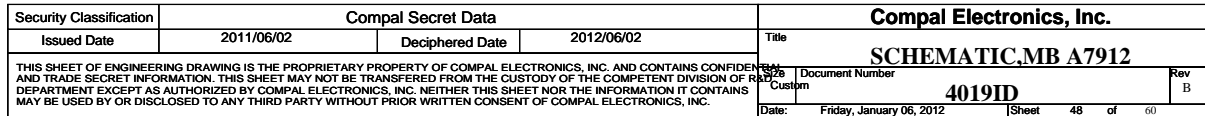


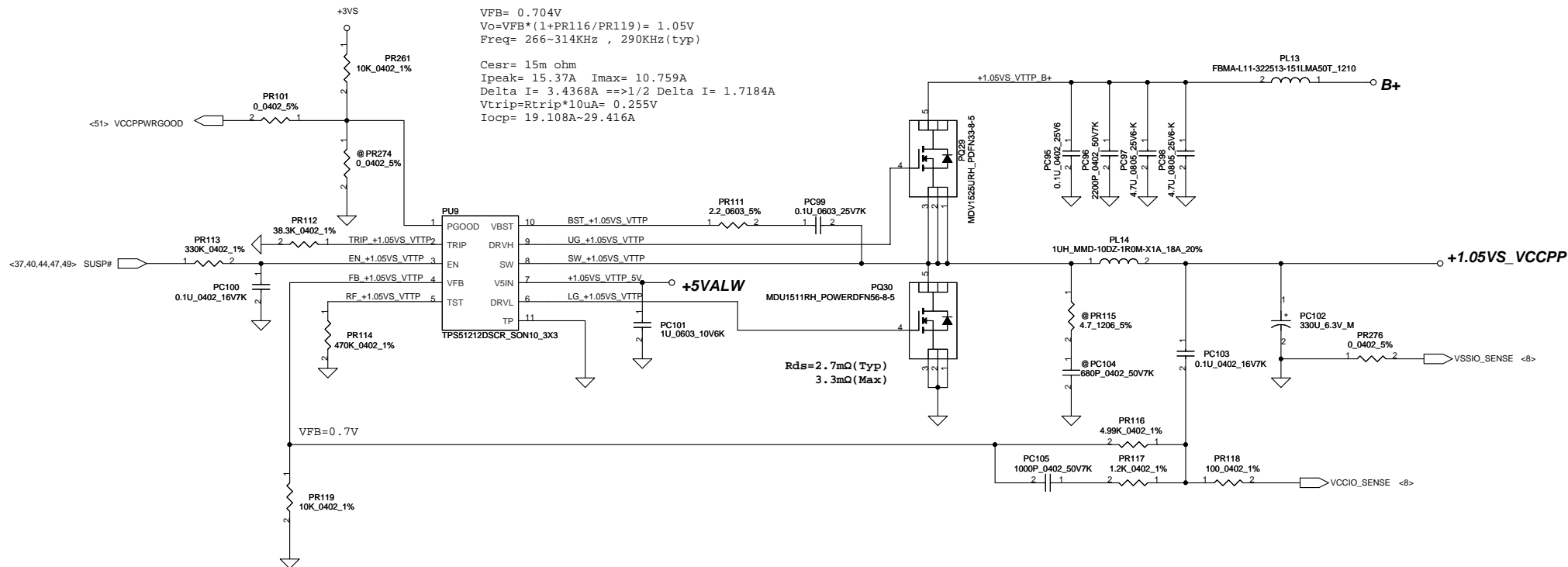
for reverse input protection

Vin Dectector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

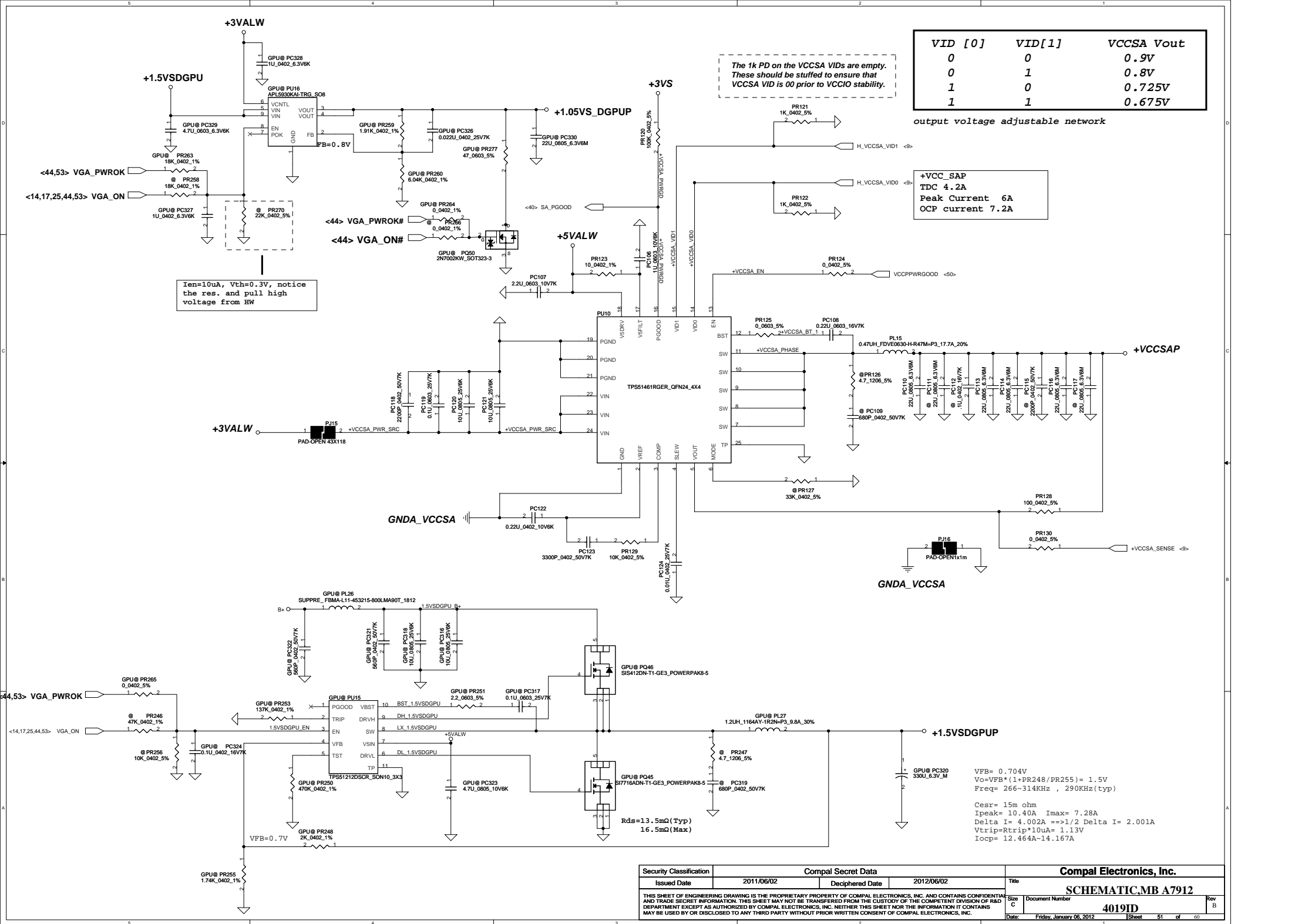
ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

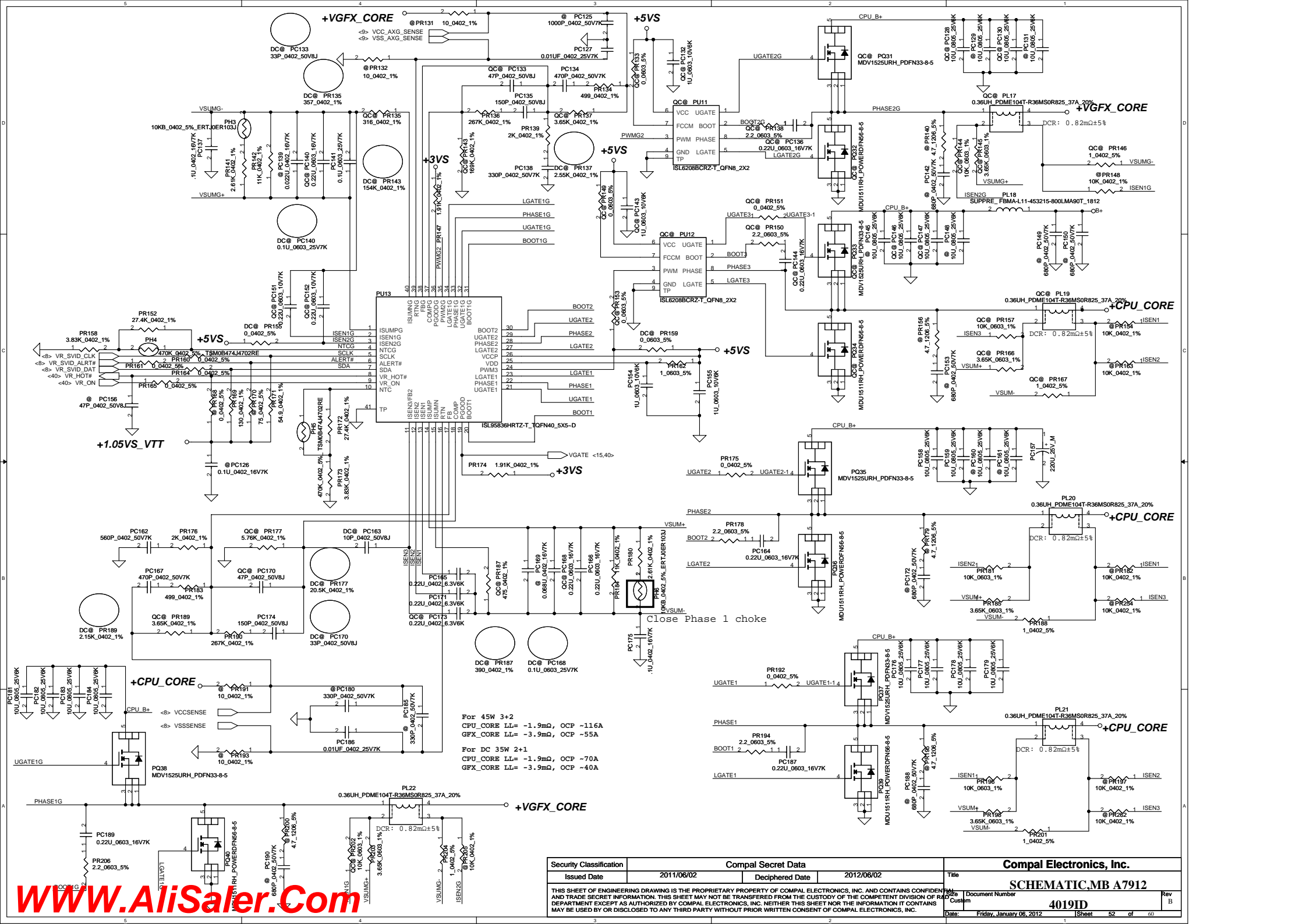
WWW.AliSaler.Com



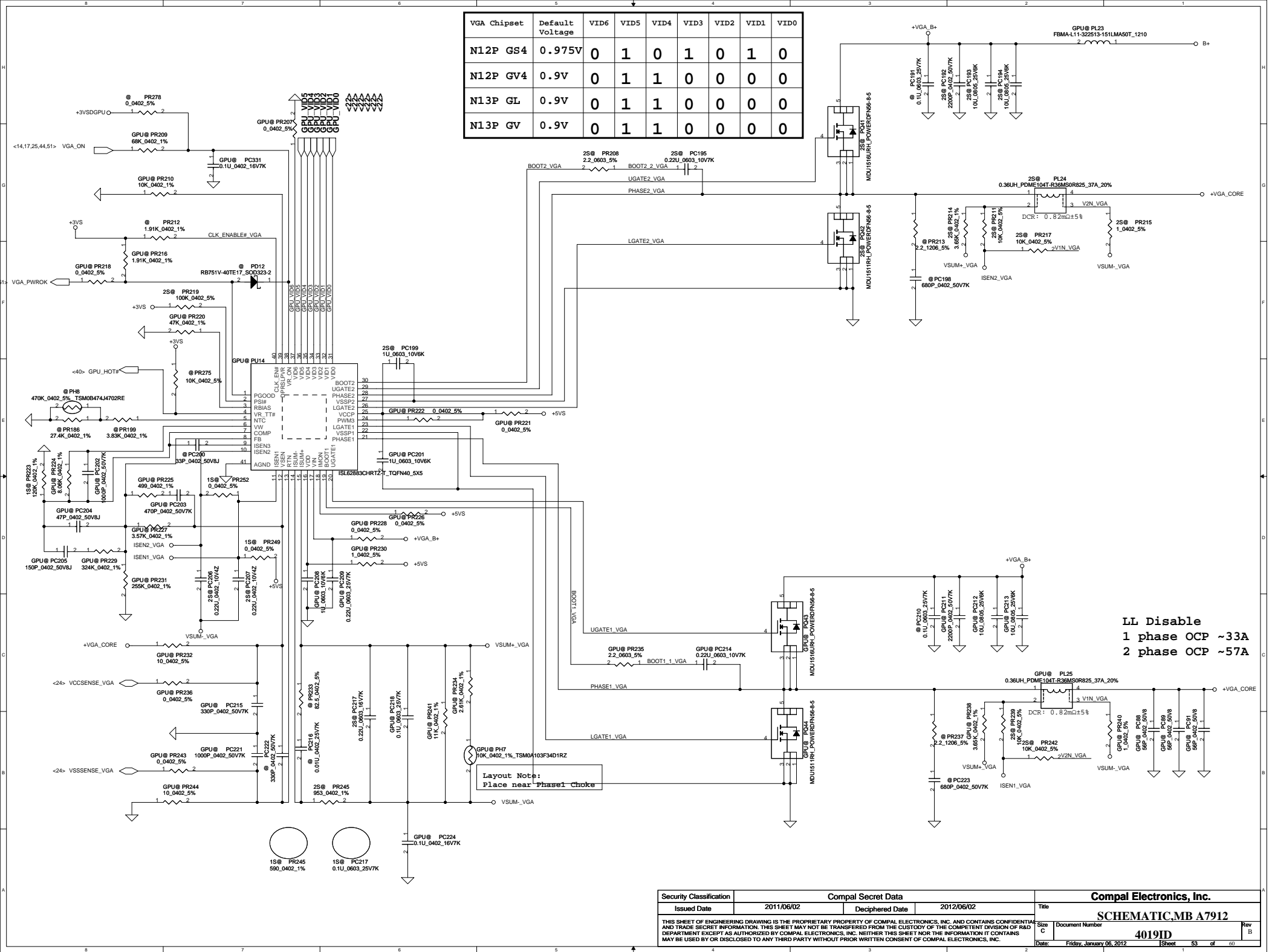


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				Document Number	40191D
				Date	Friday, January 06, 2012
				Sheet	50 of 60
				Rev	B



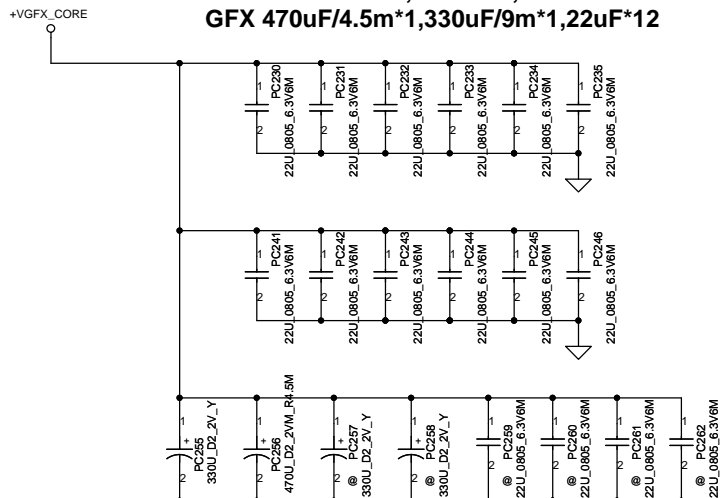


VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0



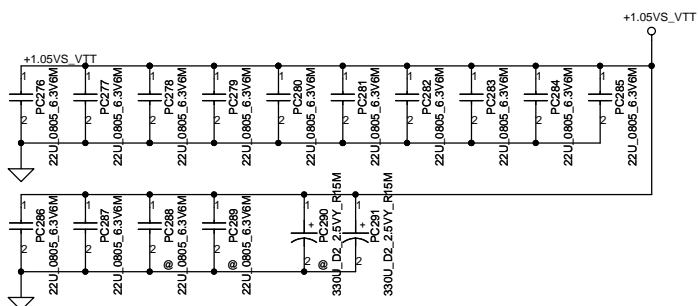
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					Size	Document Number	Rev
					C	4019ID	B
					Date:	Friday, January 06, 2012	Sheet

PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

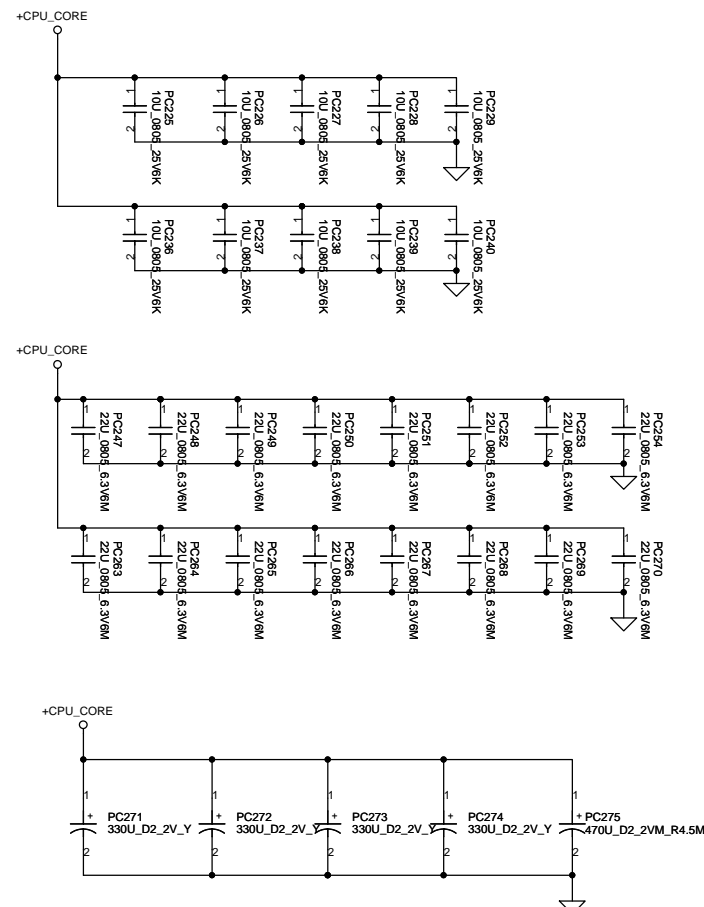


Vaxg

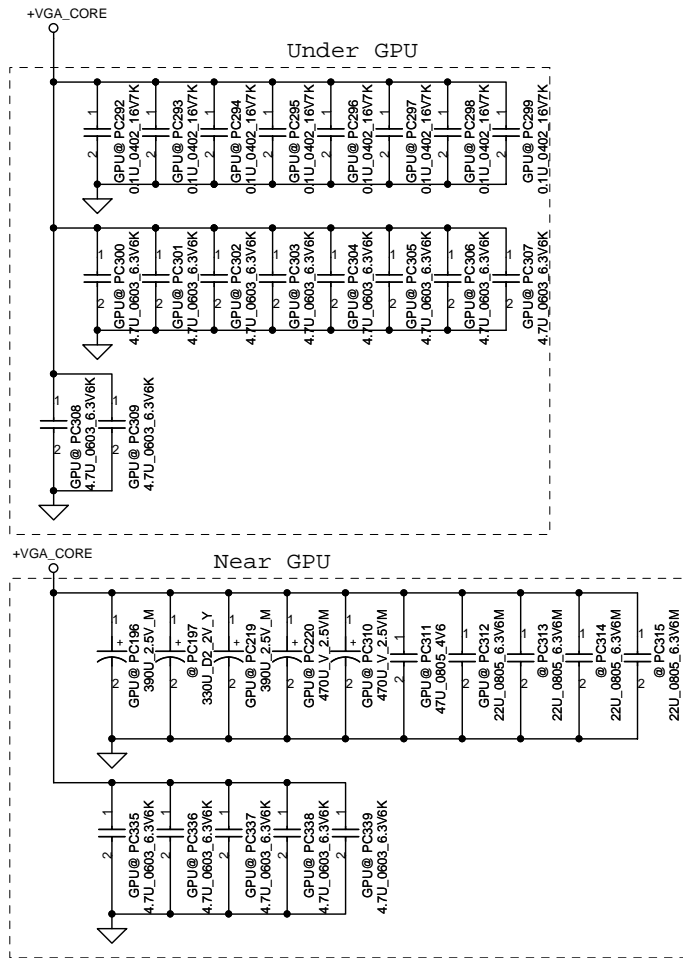
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0



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				Date	Friday, January 06, 2012
				Sheet	54 of 60



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title	SCHEMATIC, MB A7912
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				Date:	Friday, January 06, 2012
				Sheet	55 of 60

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2		
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	DVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	DVT
8							
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				4019ID
Date: Friday, January 06, 2012				Rev B
Sheet 56 of 60				

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)		0.2
7	P.44		9/7	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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				4019ID	B
Date: Friday, January 06, 2012				Sheet 58 of 60	

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088,R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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				Date: Friday, January 06, 2012	Sheet 59 of 60	

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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				Date:	4019ID	B
				Friday, January 06, 2012	Sheet 60 of 60	